SERVICE MANUAL

Zenith Local Area Network Interface Card (NET-100-1)

Z-100 Series Computers

585-49-02

860-42

ZENITH data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

Zenith Data Systems Corporation
St. Joseph, Michigan 49085

Contents

Contents

Contents

Figures

Tables

Abbreviations

ACK	Acknowledgment
ADIE	Address/Data Input Enable
AS	Address Strobe
BINP	Bus Input
BMEMR	Bus Memory
BOUT	Bus Output
BSYNC	Bus Synchronization
CE	Chip Enable
CLK	Clock
CR	Carriage Return
DBIN	Data Bus Input
DID	Destination Identification Number
DIP	Dual Inline Pack
DIS	Disable
EN	Enable
EOT	End Of Time
ESDS	Electrostatic Sensitive Devices
ET	Extended Timeout
LED	Light Emitting Diode
IDDAT	ID Data In
IDLD	ID Load
I/O	Input/Output
ILE	Interface Latch Enable
IM	Interface Module
IOADRS	Input Output Address
IOREQ	Input Output Request
ID	Identification Number
INTR	Interrupt
LANC	Local Area Network Controller
LANT	Local Area Network Transceiver
MASM	Macroassembler
MEMADRS	Memory Address
MEMREQ	Memory Request
MUX	Multiplexer
NAK	No Acknowledgment
NID	Next Identification Number
OE	Output Enable

Abbreviations

PAL	Programmable Array Logic
PR	Preset Lines
PRSFF	Preset Flip-Flop
PULS	Pulse
RAM	Random Access Memory
RDY	Ready
REQ	Request
ROM	Read Only Memory
ROMSEL	ROM Select
RX	Receive
SID	Source Identification Number
TX	Transmit
WE	Write Enable
ZLAN	Zenith Local Area Network

Specifications

Buffer RAM Size	2K × 8 (6116-4)
ROM Size Options	4K × 1 (2732-2) 8K × 8 (2764-2) 16K × 8 (27128-2)
I/O Addressing	Jumper selectable 8-bit or 16-bit addressing
Memory Addressing	Jumper selectable 16-bit or 24-bit addressing
Maximum Distance Between Units	2000 feet
Maximum Nodes Per System	255
Interrupt Operation	Jumper selectable VI0*-VI7*, NMI, and INT*
Local Area Network Controller	SMC COM9026
Local Area Network Interface	Zenith Hybrid EGA059102A
RAM/I/O Access Time	880 ns maximum
ROM Access Time	220 ns maximum
Cable Interface	RG62A Coax, 93 Ohms BNC Connector
Bus Interface	S-100, IEEE Standard 696
Power Requirements	8-11 volts DC Typical 1.6A, Maximum 2.0A −12 volts DC at .03A

Chapter 1
Introduction

This chapter introduces the NET-100-1 Card, Zenith Local Area Network (ZLAN) operation, parts supplied, and the tools required for installation.

NET-100-1 Card

The NET-100-1 Card is a local area networking card compatible with Data point's ARCNET System. It will allow the Z-100 Computer to interface with up to 255 similarly configured computers, at a maximum distance of 2000 feet. An active 4-port hub is incorporated on the NET-100-1 Card. A local area network can be set up by daisy chaining or with the hub, using the appropriate software. This card is supplied fully populated, and may be placed in any vacant card slot in the computer.

The active hub requires all units in a path or tree to be powered up for the system to communicate properly.

The card can be configured in many ways with the available switches and jumpers. This capability is especially useful for configuring the memory on the card around system memory. Yet, the card can be used as supplied, fully configured except for the ID number. The ID number is a switch set to the desired ID number. Refer to appendix A for number selection and conversion.

All of the information needed to use the features of the NET-100-1 Card is contained within this manual. Please read it carefully before attempting to use the NET-100-1 Card.

Network Operation

ZLAN consists of a token-passing scheme, where each node (unit) passes to the next active higher ID number an invitation to transmit. Up to 255 unique node numbers may be assigned to a ZLAN network (refer to Figure 1-1).

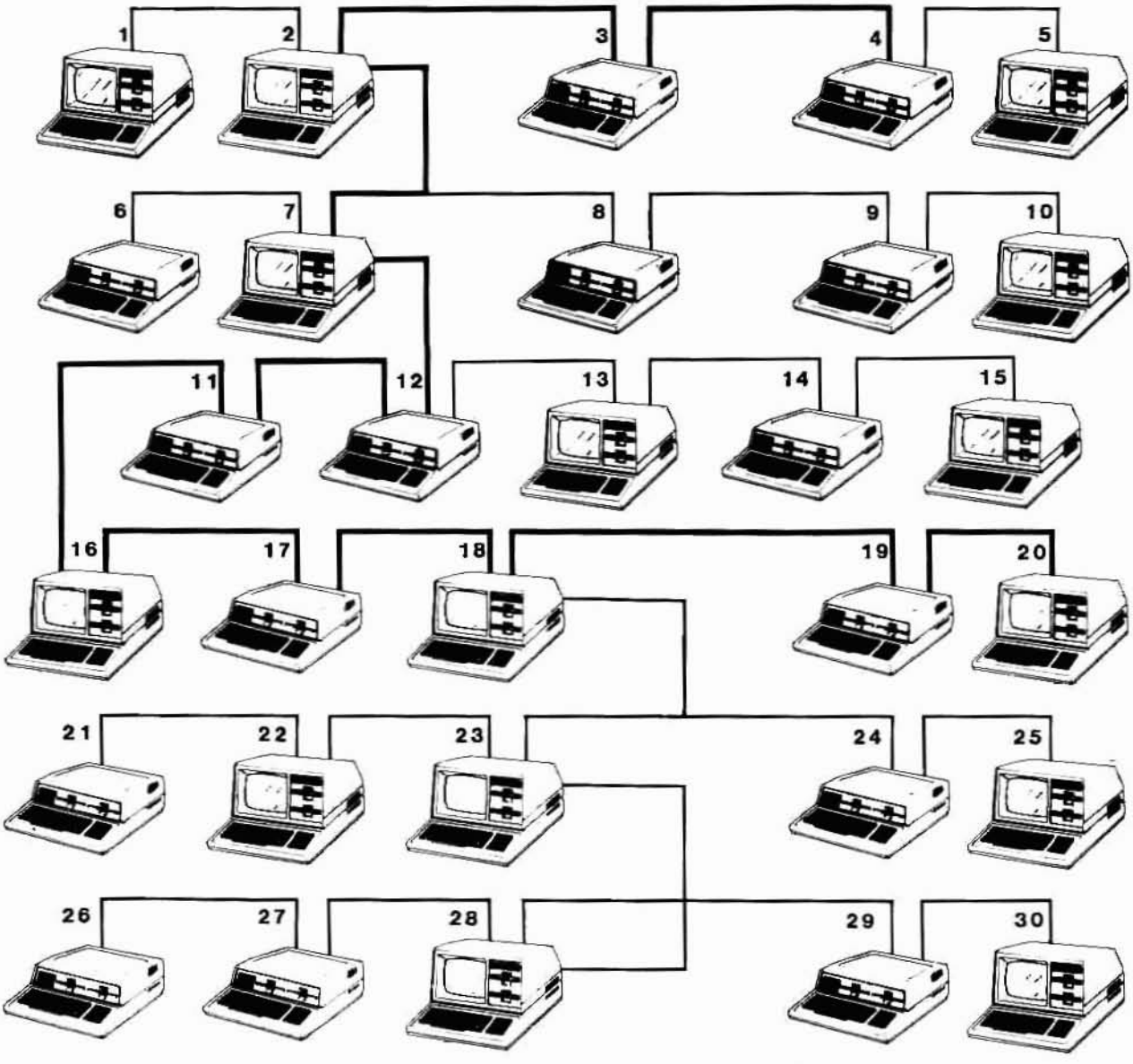


Figure 1-1. ZLAN Topology

Refer to Figure 1-1 for the following example.

EXAMPLE: Node 4 desires to communicate to node 20. The interconnecting nodes must be powered on because the board has an **active*** hub.

Nodes: 2, 3, 4, 7, 11, 12, 16, 17, 18, 19, and 20.

The network can be configured in two ways. Each has advantages and disadvantages which depend on the system to be installed. For the highest efficiency network, determine which configuration is best for the system.

Figure 1-2 shows a daisy chain configuration. The main advantage of this configuration is that a unit may be easily inserted into the system, keeping cable runs at a minimum. The disadvantage of this system is that all units must be powered on for communications to occur.

For example, a network system is set in a company where 5 of 20 units are, at times, inaccessible to the other users. Using a daisy-chain configuration, **the entire system will not be able to communicate if any unit is powered down.** Without access to 5 computers, those physical lines must be bypassed, (if this is even possible) for the network to communicate. This is an undesirable situation which can be avoided by using the tree configuration.

Figure 1-3 shows a basic tree configuration. Set up in branches, this configuration does not require all systems to be powered on for communication to occur, just the individual branch must be active. The main disadvantage is that the tree configuration does require prethought on wiring. Possible future sites should be taken into consideration while connecting the system, when using the tree configuration.

In the tree configuration, the unaccessible 5 computers can be set in a separate branch, allowing the network to communicate without these units powered on.

Although these configurations may look unique, the logical network is the same, as shown in Figure 1-4. **Do not** connect the network in this manner. Use only a daisy chain or tree configuration.

Introduction

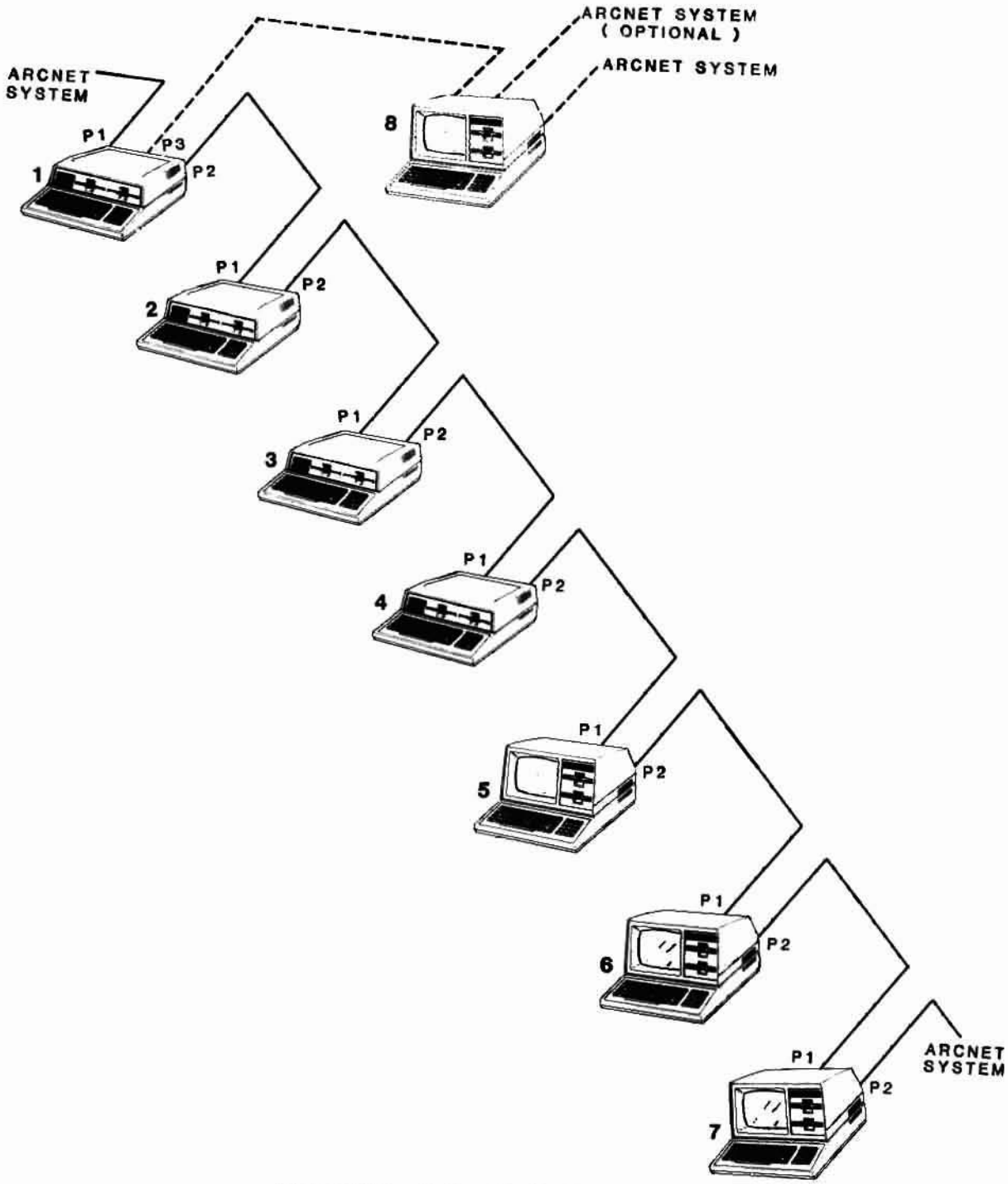


Figure 1-2. Daisy Chain Configuration

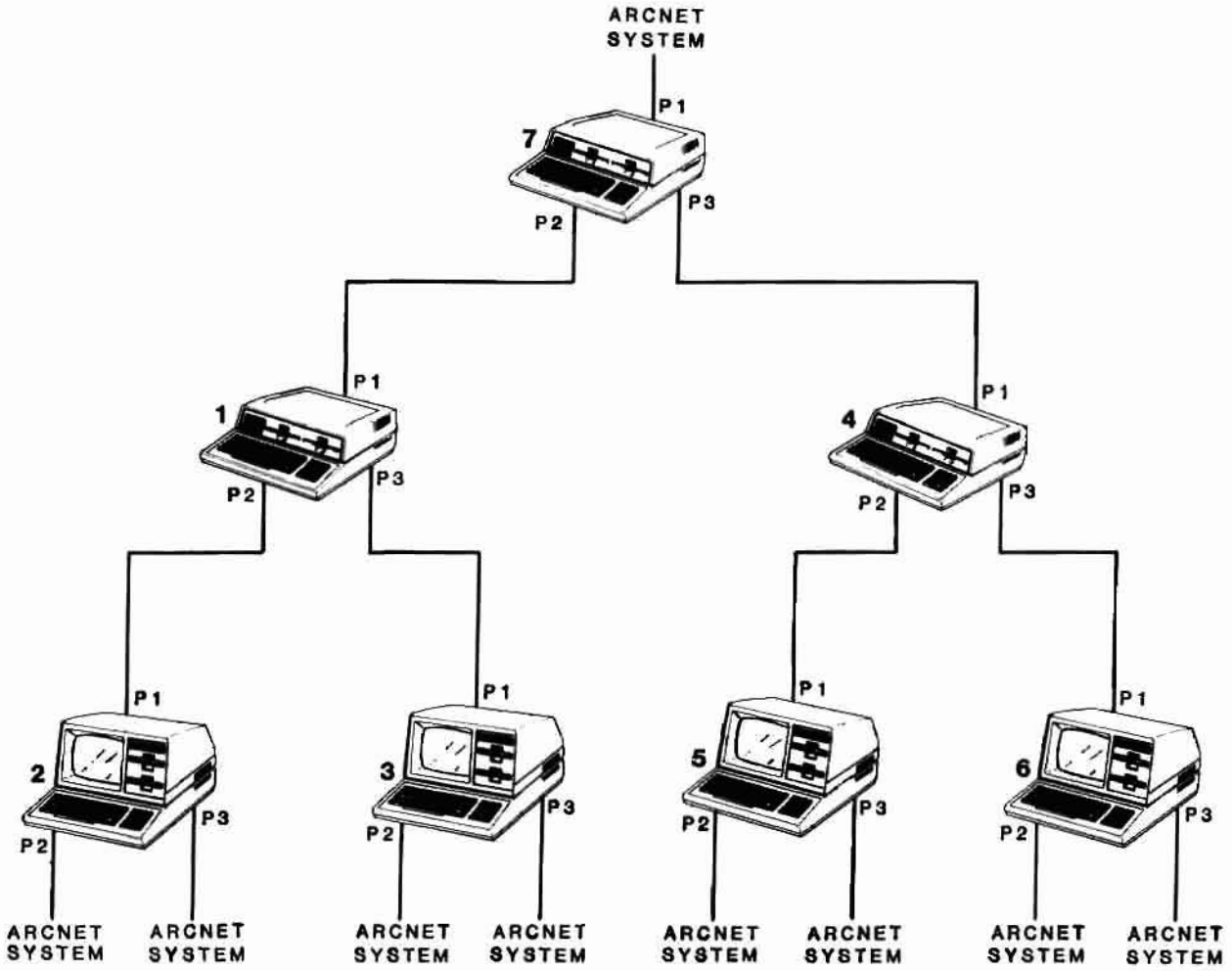


Figure 1-3. Tree Configuration

Introduction

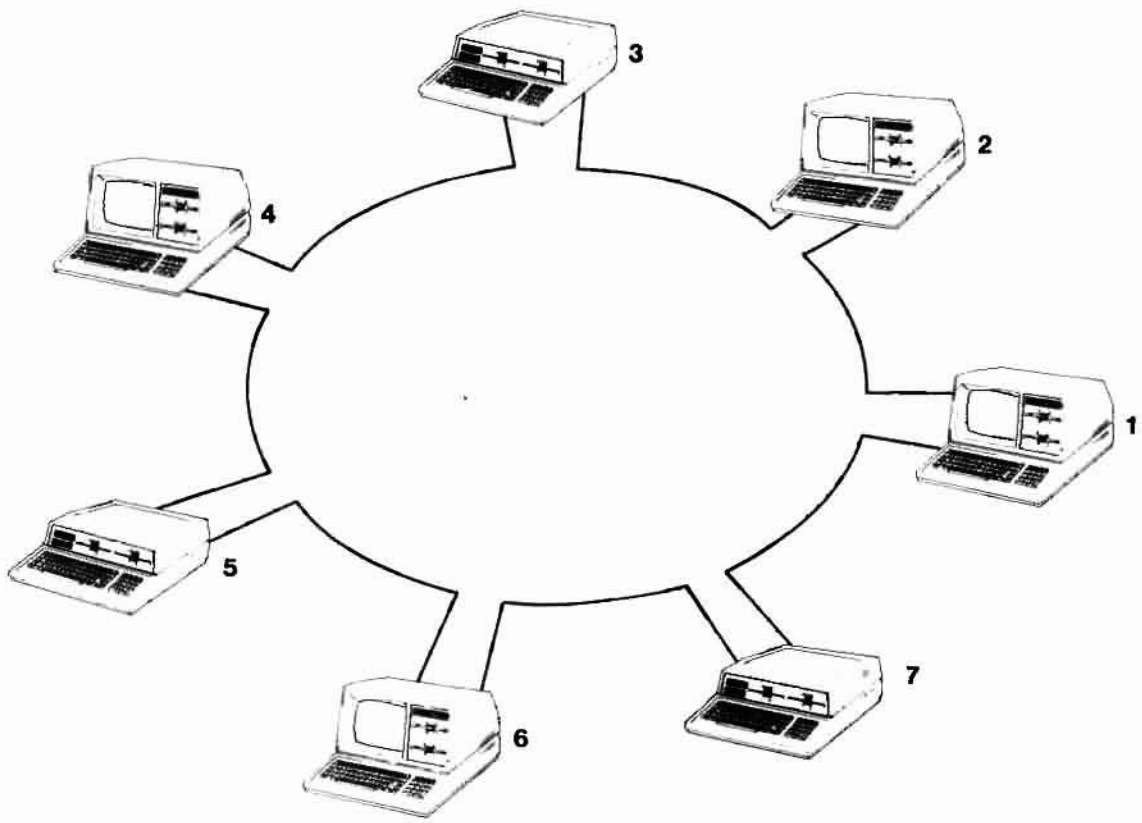


Figure 1-4. Logical Network

Network Reconfiguration

At network reconfiguration time, all ID numbers, up to 255, are polled. Each node will remember the next ID number (NID) the token was passed to. In this way, the token will be passed only to active ID numbers, preventing wasted time. Every time a node is powered up in the network, a network reconfiguration will occur. The network reconfiguration (consisting of eight marks and one space repeated 765 times) will destroy the token and prevent another node from taking control of the network.

When a node is powered down or disconnected, there is no need for a network reconfiguration. When the preceding node does not receive a response from its invitaton to transmit, it will increment the NID it has stored and send another invitation to transmit. The node will continue to increment the NID and retransmit until a response is received from an active node.

Packet Transfer

Transmit

When a node receives the token and it has a packet or message it wants to send, it looks at the destination ID (DID) and sends a free buffer inquiry to that ID (if the DID is 0, it signifies a broadcast to all nodes). If the DID responds with an acknowledge (ACK), the node will send the packet. If there is no acknowledgment (NAK) or ACK is not received after 74 microseconds, the node will pass the token to the NID.

Receive

The node receiving a free buffer inquiry checks the receiver inhibited flag. If the flag is set, an NAK is sent to the source ID (SID); if not, an ACK is sent.

When a packet is transmitted, the receiving node first writes the SID into its receive buffer. Next, it will look at the DID. If the DID is neither 0 nor its ID number, the node will ignore the rest of the packet.

If the DID corresponds to the receiving node's ID number, the node will send an ACK to the SID, set the receiver inhibited flag, and write the packet into its receiver buffer. For a broadcast (DID=0), the node will store the packet in its receive buffer if broadcast reception is enabled. If not enabled, the node will ignore the rest of the packet.

Parts Supplied

The following parts are supplied in this interface card package:

- NET-100-1 Card
- NET-100-1 Chassis Adapter
- (2) 6-BT × .375" Screws
- NET-100-1 USER'S MANUAL

The following accessories are optional:

- HCA-60 — 25 foot coax cable.
- HCA-61 — 100 foot coax cable.

Tools Required

The only tools required for the installation of the NET-100-1 Card are a small flat blade screwdriver and a small Phillips screwdriver.

Chapter 2

Hardware and Host Computer Requirements

Introduction

The NET-100-1 Card uses the S-100 Bus Interface, IEEE Standard 696. Therefore, computers used with this card must meet the same standard. Listed below are the S-100 Bus pins used, signal, type, and their active level.

S-100 Bus Pin

PIN NO.	SIGNAL/TYPE	ACTIVE LEVEL
4	VI0* (S)	L O.C. (Low open collector)
5	VI1* (S)	L O.C.
6	VI2* (S)	L O.C.
7	VI3* (S)	L O.C.
8	VI4* (S)	L O.C.
9	VI5* (S)	L O.C.
10	VI6* (S)	L O.C.
11	VI7* (S)	L O.C.
12	NMI* (S)	L O.C.
15	A18 (M)	H
16	A16 (M)	H
17	A17 (M)	H
20	GND (B)	0 Volts Line
24	OI (B)	H
29	A5 (M)	H
30	A4 (M)	H
31	A3 (M)	H
32	A15 (M)	H
33	A12 (M)	H
34	A9 (M)	H
35	DO1 (M) /DATA1 (M/S)	H
36	DO0 (M) /DATA0 (M/S)	H
37	A10 (M)	H
38	DO4 (M) /DATA4 (M/S)	H
39	D05 (M) /DATA5 (M/S)	H
40	DO6 (M) /DATA6 (M/S)	H
41	DI2 (M) /DATA10 (M/S)	H

Hardware and Host Computer Requirements

PIN NO.	SIGNAL/TYPE	ACTIVE LEVEL
42	DI3 (M) /DATA11 (M/S)	H
43	DI7 (M) /DATA15 (M/S)	H
45	sOUT (M)	H
46	sINP (M)	H
47	sMEMR (M)	H
50	GND (B)	0 Volts Line
51	+8 Volts (B)	
52	−16 Volts (B)	
53	GND (B)	0 Volts Line
59	A19 (M)	H
61	A20 (M)	H
62	A21 (M)	H
63	A22 (M)	H
64	A23 (M)	H
67	PHANTOM* (M/S)	L O.C.
70	GND (B)	0 Volts Line
72	RDY (S)	H O.C.
73	INT* (S)	L O.C.
75	RESET* (B)	L O.C.
76	pSYNC (M)	H
77	pWR* (M)	L
78	pDBIN (M)	H
79	A0 (M)	H
80	A1 (M)	H
81	A2 (M)	H
82	A6 (M)	H
83	A7 (M)	H
84	A8 (M)	H
85	A13 (M)	H
86	A14 (M)	H
87	A11 (M)	H
88	DO2 (M) /DATA2 (M/S)	H
89	DO3 (M) /DATA3 (M/S)	H
90	DO7 (M) /DATA7 (M/S)	H
91	DI4 (S) /DATA12 (M/S)	H
92	DI5 (S) /DATA13 (M/S)	H
93	DI6 (S) /DATA14 (M/S)	H
94	DI1 (S) /DATA9 (M/S)	H
95	DI0 (S) /DATA8 (M/S)	H
96	sWO* (M)	L
100	GND (B)	0 Volts Line

Chapter 3
Disassembly

Introduction

This chapter provides the information to remove the top of the Z-100 Computer for NET-100-1 Card installation.

WARNING: Dangerous DC voltages are present inside the computer. Be sure the line cord is disconnected.

Disassembly

All-in-One Model — Refer to Figure 3-1 and complete the following steps.

1. Unplug the line cord from the AC outlet.
2. Using a small flat blade screwdriver, move the metal slides all the way to the front and then 1/4" to the back as shown.
3. Carefully lift the top case straight up and set it to one side.

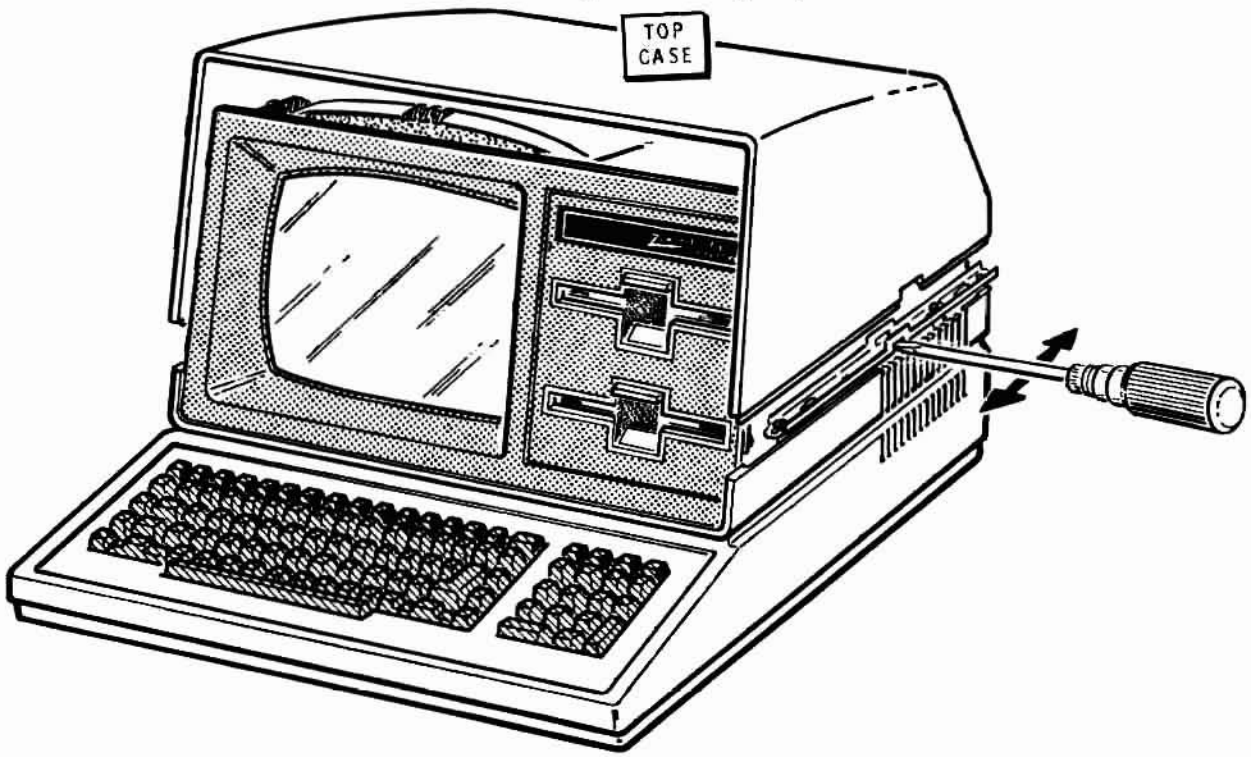


Figure 3-1. Disassembly, All-in-One Model

Disassembly

Low-Profile Model — Refer to Figure 3-2 and complete the following steps.

1. Unplug the line cord from the AC outlet.
2. Pull the metal slides all the way to the back, and then push the metal slides 1/4" to the front, as shown.
3. Carefuly lift the top case straight up and set it to one side.

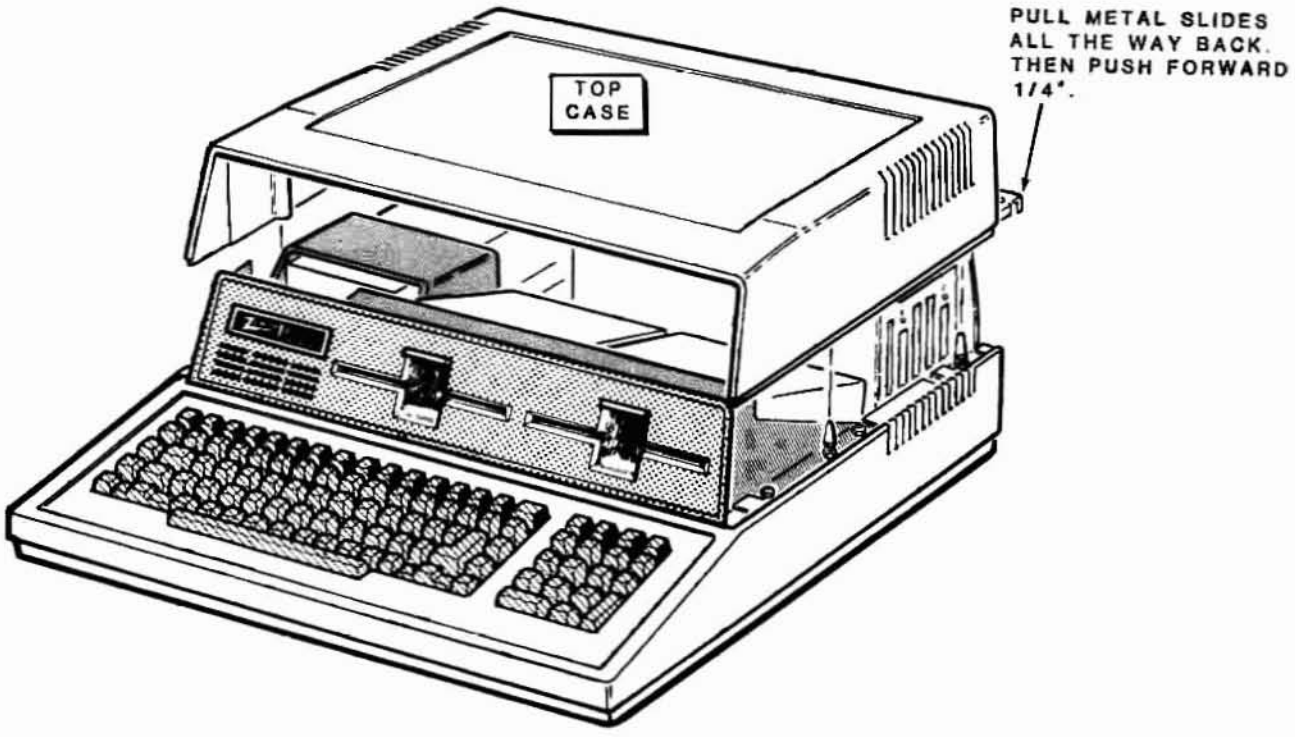


Figure 3-2. Disassembly, Low-Profile Model

Chapter 4
Configuration

Introduction

This chapter describes the typical factory configuration used with the Z-100 Computer. Detailed configuration information is furnished for Z-100 users who desire to modify or customize their configuration, and non-Zenith Data System microcomputers with S-100 Bus compatiblity.

Typical Configuration

The following is the typical board configuration which is preset at the factory. Refer to Figure 4-1 while reading this section.

CAUTION: This product contains ESDS (electrostatic sensitive) devices. Exercise normal caution in handling these devices to prevent static discharge damage.

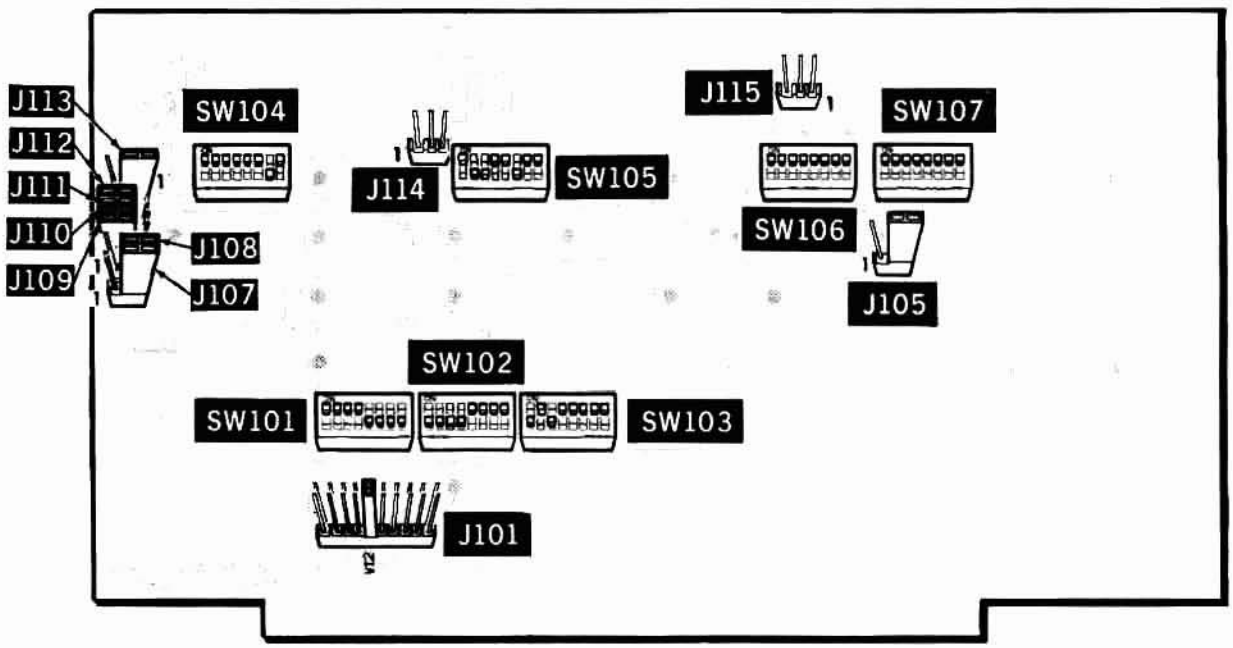


Figure 4-1. Typical Configuration

Configuration

- Programming jumper across J101, pin 5 (VI2* interrupt).
- Programming jumper on J105, pins 2 and 3 (right) (8-bit I/O addressing).
- Programming jumper on J107 and J108, pins 2 and 3 (right), and J109, J110, and J111, pins 1 and 2 (left) (test points on COM9026 chip).
- Programming jumper on J112, pins 1 and 2 (left), and J113, pins 2 and 3 (right) (2764-2 ROM).
- DIP (Dual Inline Pack) Switch SW101 positions 0 – 3 to the ON (0) position and all others to the OFF (1) position to select 0F0000H for the RAM address.
- DIP Switch SW102 positions 0, 1, 2 and 3 to the OFF (1) position and all others to the ON (0) position to select 0F4000H for the ROM address.
- DIP Switch SW103 positions 0 and 2 to the OFF (1) position and all others to the ON (0) position to select 00A0H for the I/O address.
- Dip Switch SW104 position 6 to the OFF(1) position and all other positions to the ON (0) position.
- DIP Switch SW105 is the ID number switch. Set this to the ID number you desire. (Each unit in the system must have a unique ID number.) For example, for ID number 100 (64H), set positions 1, 2 and 5 to the OFF (1) position and all others to the ON (0) position, as shown. Refer to appendix A for cross reference to other ID numbers and their respective positions.

POSITION	0	1	2	3	4	5	6	7
ON/OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON

NOTE: To insure proper setting refer to memory test in Chapter 6.

- Dip Switch SW106 all positions to the ON (0) position.
- Dip Switch SW107 all positions to the ON (0) position.

Detailed Configuration Data

The following information is furnished to configure the NET-100-1 Card for non-Zenith Data System S-100 Bus compatible microcomputers, as well as for the Z-100 user who desires to make modifications or effect a customized configuration.

CAUTION: This product contains ESDS (electrostatic sensitive devices). Exercise normal caution in handling these devices to prevent static discharge damage.

Refer to Figure 4-2 for the locations of the jumpers.

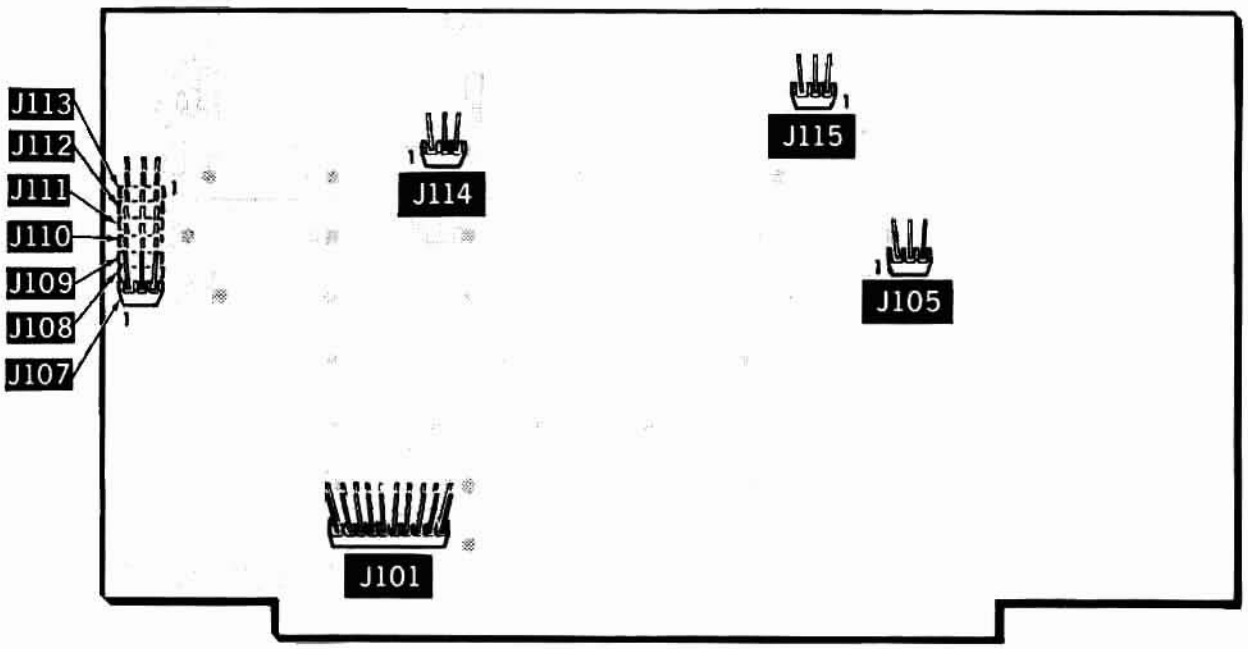


Figure 4-2. Configuration Jumpers

Configuration

Jumpers

J101 — Selects the interrupt on the S100 Bus. Only one of the following should be jumpered.

NMI*
INT*
VI0*
VI1*
VI2*
VI3*
VI4*
VI5*
VI6*
VI7*

J105 — For 16-bit addressing pins 1 and 2 are jumpered; for 8-bit addressing, pins 2 and 3 are jumpered.

J107 (T2) — Jumper pins 2 and 3 for normal COM9026 operation. When pins 1 and 2 are jumpered, chip level testing can be performed.

J108 (T1) — Jumper pins 2 and 3 for normal COM9026 operation. When pins 1 and 2 are jumpered, chip level testing can be performed.

J109 (ECHO) — Jumper pins 1 and 2 for normal COM9026 operation. When pins 2 and 3 are jumpered, COM9026 will retransmit **all** messages less than 254 bytes.

J110, J111 — These two jumpers specify the time-out durations as follows:

ET2	ET1	RESPONSE TIME (us)	RECONFIGURATION TIME (ns)
1	1	74.7	840
1	0	283.4	1680
0	1	561.8	1680
0	0	1118.6	1680

J112 — When using a 27128 ROM, jumper pins 2 and 3. For other size ROM's, jumper pins 1 and 2.

J113 — When using a 2732 ROM, jumper pins 1 and 2. For 2764 or 27128, jumper pins 2 and 3.

J114 — When pins 2 and 3 are jumpered, the EPROM will not cause PHANTOM* to be active. When pins 1 and 2 are jumpered, PHANTOM* will be active when the ROM is selected.

J115 — When using a 2732 ROM, jumper pins 2 and 3. For a 27128, jumper pins 1 and 2. For a 2764, no jumper is required.

Switches

Refer to Figure 4-3 for the location of the switches. In the following configurations, OFF equates to a logic "1", and ON to a logic "0".

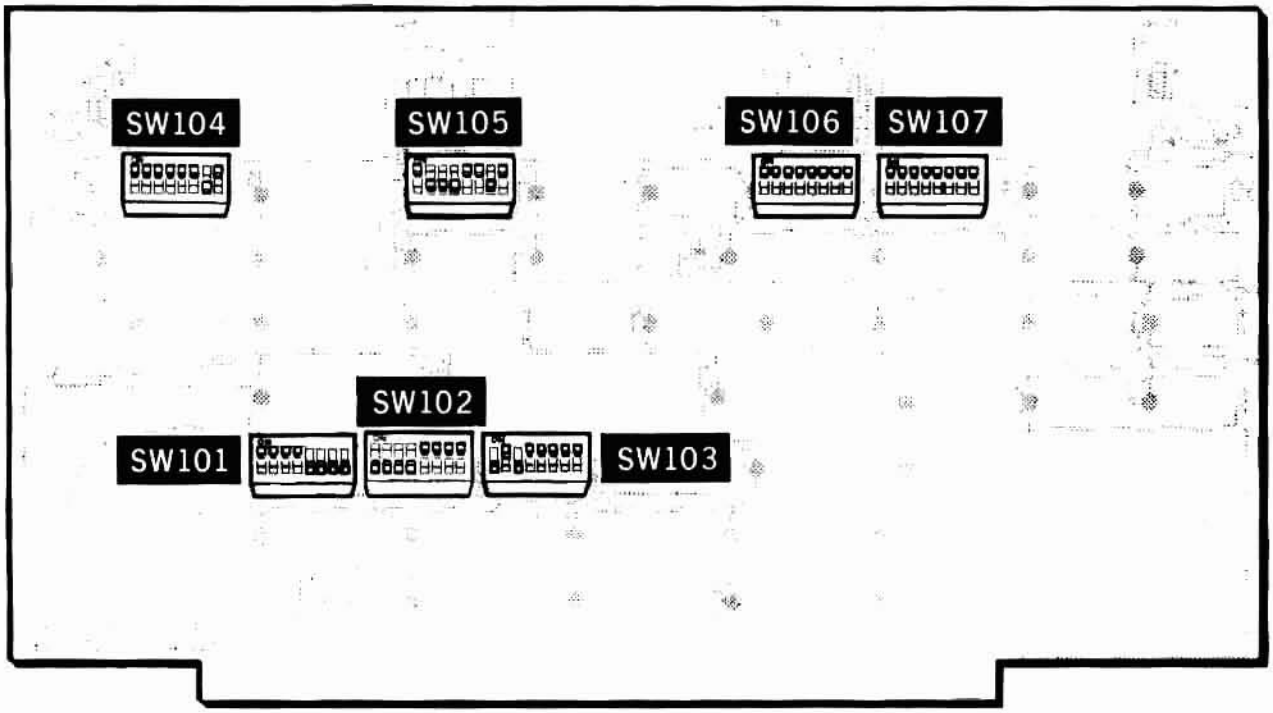


Figure 4-3. Configuration Switches

Configuration

SW101 — This switch, in conjunction with SW106, selects the memory address location for the RAM. For example, to select the address 0F000 (HEX), SW101 would have the following configuration:

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A23	A22	A21	A20	A19	A18	A17	A16
ON/OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF

SW102 — This switch, in conjunction with SW104, selects the location of the ROM. For example, to select the address 0F4000 (Hex), SW104 would have the following configuration:

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A16	A17	A18	A19	A20	A21	A22	A23
ON/OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON

SW103 — This switch, in conjunction with SW107, selects the I/O address location. For example, to select 00A0 (HEX), SW107 would have the following configuration:

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A7	A6	A5	A4	A3	A2	A1	NC
ON/OFF	OFF	ON	OFF	ON	ON	ON	ON	X

SW104 — This switch, in conjunction with SW102, selects the location of the ROM, 0F4000; SW104 would have the following configuration:

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	NC	NC	NC	NC	NC	A15	A14	A13
ON/OFF	X	X	X	X	X	ON	OFF	ON

SW105 — This switch selects the ID node number. There should be a unique node number for every unit in the network. When position 7 is set OFF and all other positions ON, the ID node number is 1. When position 6 is set OFF and all other positions ON, the node number is 2, etc. The following settings will select ID node number 114 (72H):

POSITION	0	1	2	3	4	5	6	7
ON/OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON

NOTE: This 114 number is different from the typical configuration to provide another example of ID number selection.

NOTE: To insure proper setting refer to memory test in Chapter 6.

SW106 — This switch, in conjunction with SW101, selects the MEMADRS location, 0F0000H.

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A15	A14	A13	A12	A11	NC	NC	NC
ON/OFF	ON	ON	ON	ON	ON	X	X	X

SW107 — This switch, in conjunction with SW103, selects the IOADRS location.

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A8	A9	A10	A11	A12	A13	A14	A15
ON/OFF	ON	ON	ON	ON	ON	ON	ON	ON

Chapter 5
Installation

Introduction

This chapter provides the necessary information to install the NET-100-1 Card and Network Interface.

NET-100-1 Card Installation

CAUTION: This product contains ESDS (electrostatic sensitive devices). Exercise extreme care in handling these devices to prevent damage.

Refer to Figure 5-1 and complete the following steps.

1. Select a vacant card slot in the card cage assembly.
2. Disconnect 8 inch disk drive cable (134-1264), if used.
3. Insert the NET-100-1 Card, with the components facing forward, into the selected card slot. Seat the card firmly by pushing straight down.

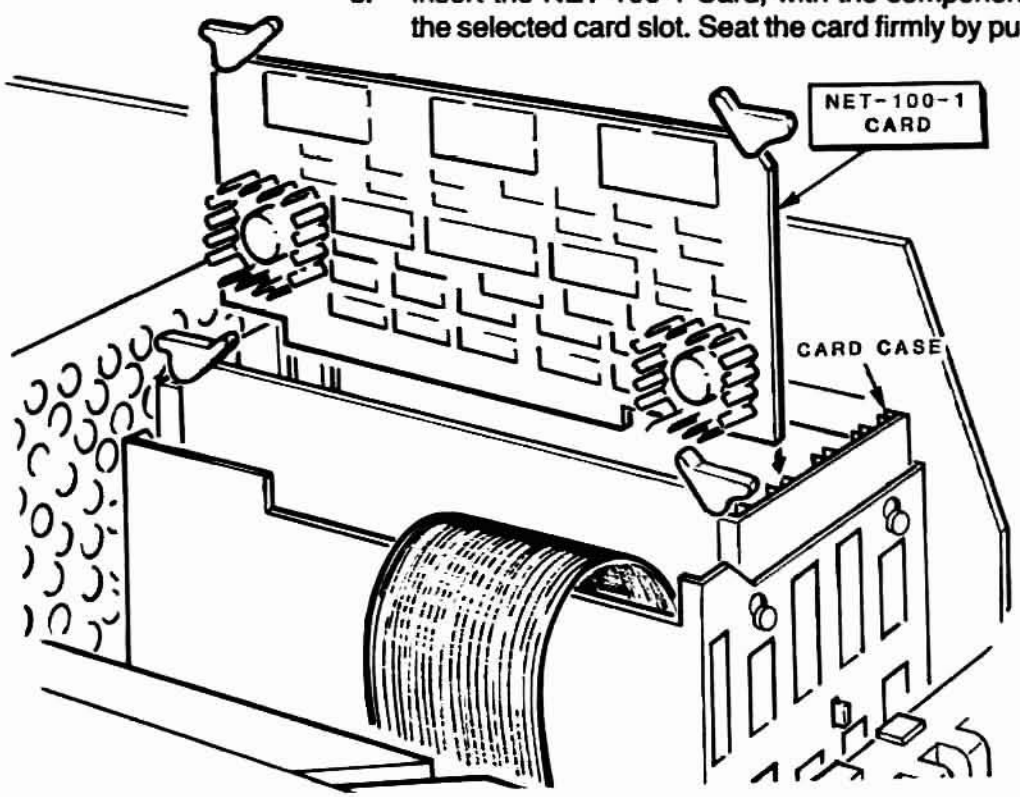


Figure 5-1. NET 100-1 Card Installation

Network Chassis Adapter Installation

Refer to Figure 5-2 and complete the steps below.

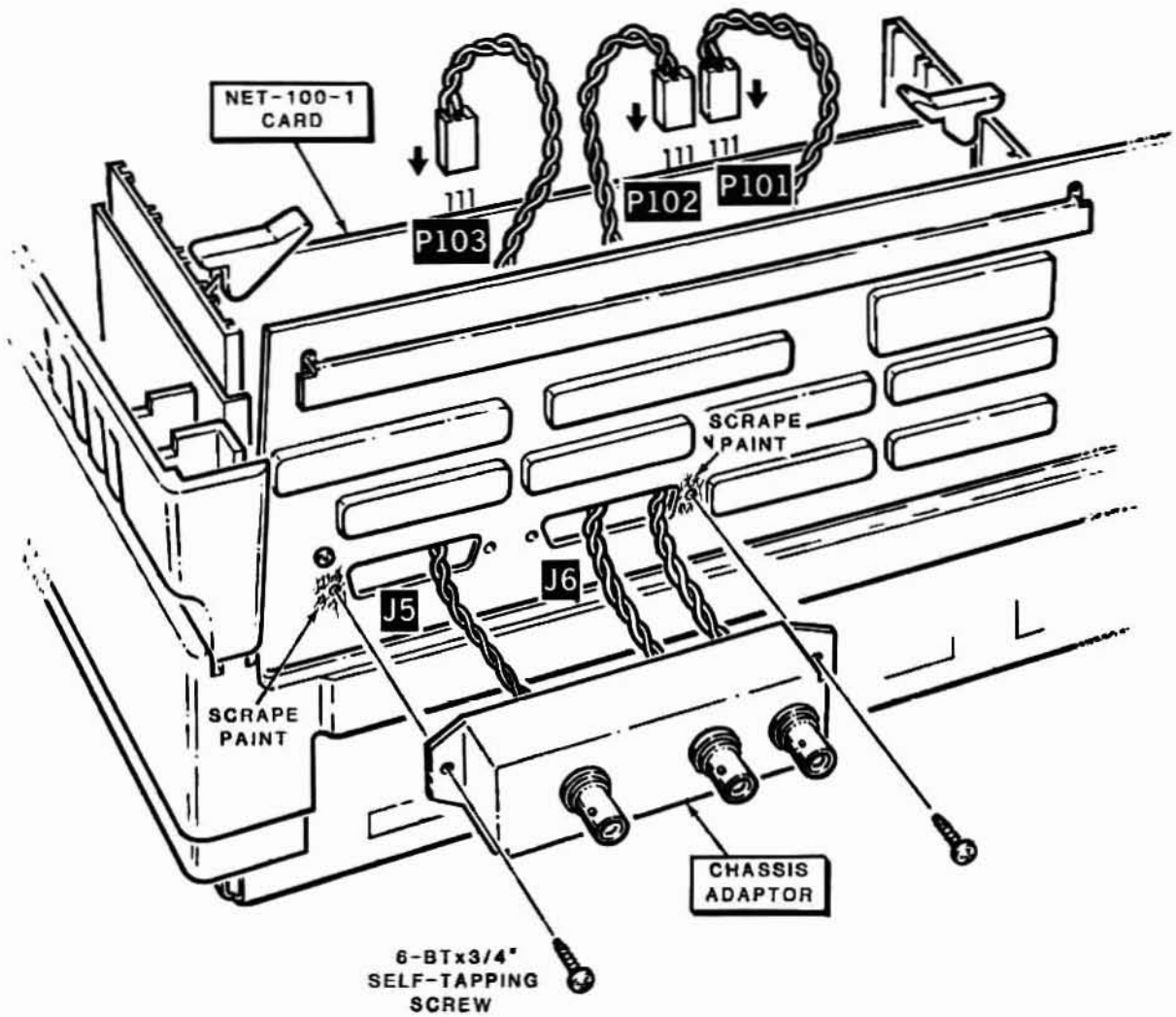


Figure 5-2. Network Chassis Adapter Installation

1. Choose two of the adjacent unused 25 D-pin connectors on the back panel. We suggest J5 and J6 connectors. Remove the hole plug buttons which cover these holes and discard them.

2. Carefully sand or scratch the paint off the back panel from the two outermost screw holes.

3. Place chassis adapter over these holes and feed the cables through the holes to the inside of the unit.

4. Using two HE 250-1434 (6-BT × .375) self-tapping screws, fasten the chassis adapter to the rear panel.

5. Connect the cables fed to the inside of the unit to the NET- 100 board connectors P101, P102, and P103. The connector has three pins, but only two contacts are used. The outer pins contain the same signal and the contact may be installed either way, as long as the middle pin makes contact with the middle connector.

This completes the installation of the network chassis adapter. To connect nodes together, RG62 coaxial cable can be run through ceilings, on floors, or along the walls. For shorter delays and less cabling, keep long runs to a minimum.

CAUTION: Since other installations may use similar cable and connectors, be sure the correct connectors and cabling are connected to the Network Chassis Adapter. Damage to this board may result if improper connections are made.

Chapter 6
Initial Tests

Introduction

This chapter contains three initial tests to make sure the NET-100-1 Card is properly operating and interfaced to the system. The three tests are RAM, I/O, and Memory.

NOTE: These tests are interrupted by pressing the CTRL and RESET keys simultaneously.

RAM Test

The following is a test routine to determine if the RAM is operating properly. Using a work processor program or EDLIN, enter the following under file RAM.ASM.

```
NET_MEM_ADRS        EQU         0F000H
DGROUP              GROUP       DSEG, STACK
CGROUP              GROUP       CSEG
                    ASSUME      CS:CGROUP, DS:DGROUP, SS:DGROUP, ES:NOTHING
DSEG                SEGMENT
DATA_BUFFER_0       DB          0, 0, 0FFH
DSEG                ENDS
STSEG               SEGMENT     STACK
                    DB          256 DUP ( ? )
STSEG               ENDS
CSEG                SEGMENT
INIT_MEMTST:
                    PUSH        AX
                    PUSH        BX
                    PUSH        CX
                    PUSH        DX
                    MOV         AX, DGROUP
                    MOV         DS, AX
INIT_BUFFER:
                    MOV         AX, NET_MEM_ADRS
                    MOV         ES, AX
                    MOV         BX, 0
                    MOV         AL, 0
```

Initial Tests

```
LOOP:
                    MOV         ES:[BX], AL
                    JMP         LOOP
                    POP         DX
                    POP         CX
                    POP         BX
                    POP         AX
                    RET
CSEG                ENDS
                    END
```

```
Type    MASM    RAM.ASM
Type    LINK    RAM
Type    RAM
```

LED D105 should light while this test is being performed. If LED D105 does not light, refer to Chapter 10, Service Instructions.

I/O Test

The following is a test routine to determine if the I/O network is operating properly. Using a word processor program or EDLIN, enter the following under file IO.ASM.

```
NET_IO_ADRS         EQU         000A0H
DGROUP              GROUP       DSEG, STACK
CGROUP              GROUP       CSEG
                    ASSUME      CS:CGROUP, DS:DGROUP, SS:DGROUP, ES:NOTHING
STSEG               SEGMENT     STACK
                    DB          256 DUP (?)
STSEG               ENDS
CSEG                SEGMENT
INIT_NET:
                    PUSH        AX
                    PUSH        BX
                    PUSH        CX
                    PUSH        DX
                    MOV         AX, DGROUP
                    MOV         DS, AX
```

```
LOOP_TRANSMIT:
LOOP_TA_0:
                    MOV         DX, NET_IO_ADRS
                    IN          AL, DX
                    AND         AL, 01
                    CMP         AL, 0
                    JE          LOOP_TA_0
                    MOV         DX, NET_IO_ADRS + 1
                    MOV         AL, 003H
                    JMP         LOOP_TRANSMIT
                    POP         DX
                    POP         CX
                    POP         BX
                    POP         AX
                    RET
CSEG                ENDS
                    END
```

```
Type    MASM   IO.ASM
Type    LINK   IO
Type    IO
```

LED D102 should light while this test is being performed. If LED D102 does not light, refer to Chapter 10, Service Instructions.

Memory Test

The purpose of this test is to determine if the RAM and its interface to the system are operating properly. If a difficulty is encountered while this test is being performed, refer to Chapter 10, Service Instructions.

1. Turn on the computer and monitor.

2. After the prompt type EF000:0 (the monitor will show Examine F000:0) **RETURN**.

   The following should be displayed on the monitor:
   F000:0000 D1 = **RETURN**

Initial Tests

Now F000:0001 64 = should be displayed, or the ID node number set by SW105 in Hex. This number will differ depending on the ID number your board is set for. **RETURN**

3. When the memory location is given on the screen, type the number listed below. After every entry hit a carriage return to advance to the next memory location.

ONSCREEN	TYPE
F000:0002	1
F000:0003	2
F000:0004	3
F000:0005	4
F000:0006	5
F000:0007	6
F000:0008	7
F000:0009	8
F000:000A	9
F000:000B	A
F000:000C	B
F000:000D	C
F000:000E	D
F000:000F	E
F000:0010	F

4. Hit the DELETE key to get the prompt back.

5 Type DF000:0-10 **RETURN**.

The following should be displayed, indicating that the RAM can be written to and read from.

```
F000:0000 D1 64 01 02 03 04 05 06 ; 07 08 09 0A 0B 0C 0D 0E
F000:0010 0F
```

NOTE: F000:0001 should read the ID node number in hex set by SW105.

Chapter 7
Reassembly

Introduction

This chapter contains the information required to install the top of the Z-100 Computer after NET-100-1 Card installation, configuration, and tests.

Reassembly

All-in-One Model — Refer to Figure 7-1. Connect cable (134-1264), if using 8-inch disk drive. Replace the top case by bringing it straight down into its position. Using a small flat blade screwdriver, slide the latches all the way to the front.

This completes the reassembly of the all-in-one model.

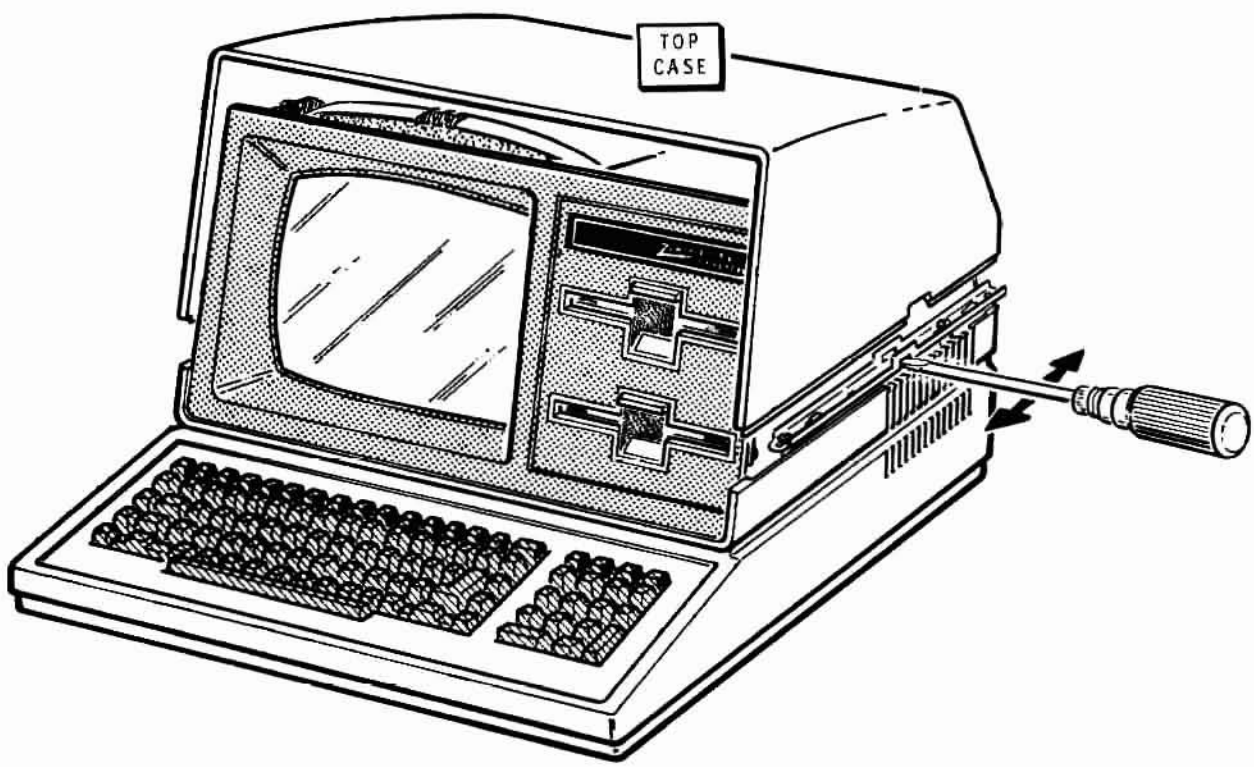


Figure 7-1. Reassembly, All-in-One Model

Reassembly

Low-Profile Model — Refer to Figure 7-2. Connect cable (134-1264), if using 8-inch disk drive. Replace the top case by bringing it straight down into its position. Push the latches all the way to the front.

This completes the reassembly of the low-profile model.

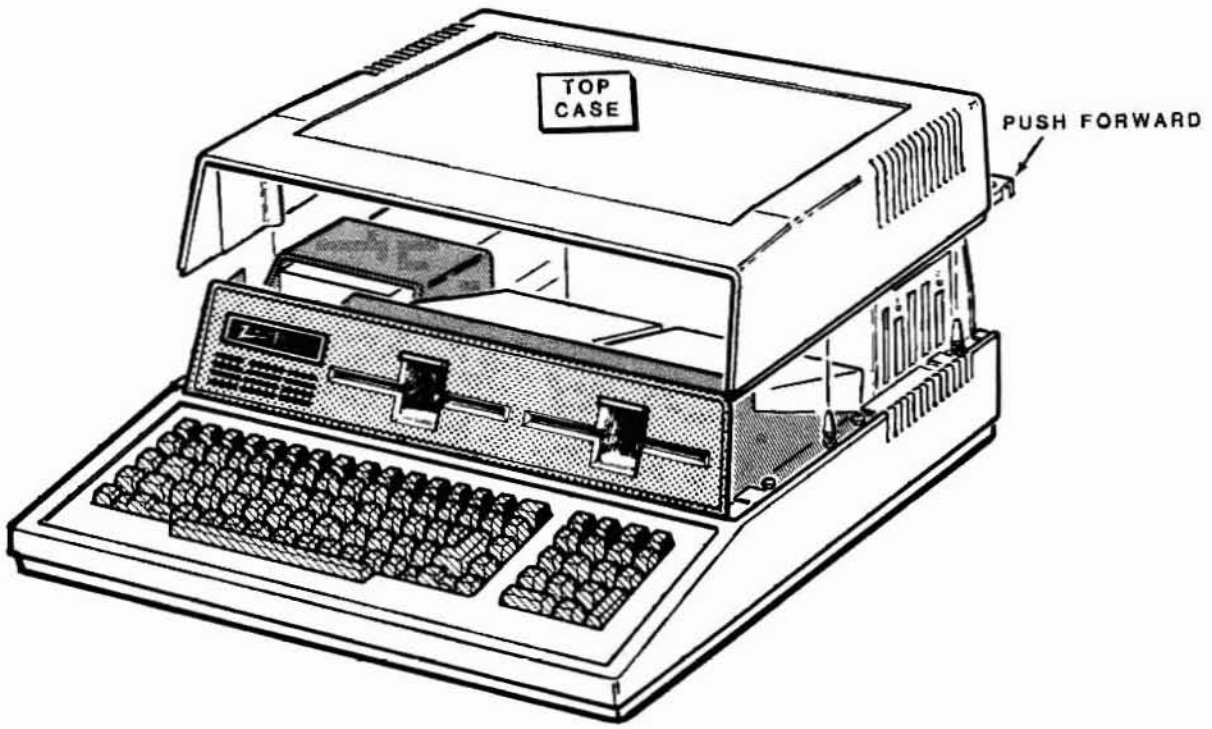


Figure 7-2. Reassembly, Low-Profile Model

Chapter 8

Theory of Operation

Introduction

This chapter provides a brief explanation of the theory of operation of the NET-100 Card. If a more detailed theory of operation is desired, refer to Chapter 9, Circuit Description. Refer to the block diagram, Figure 8-1, as you read the following description.

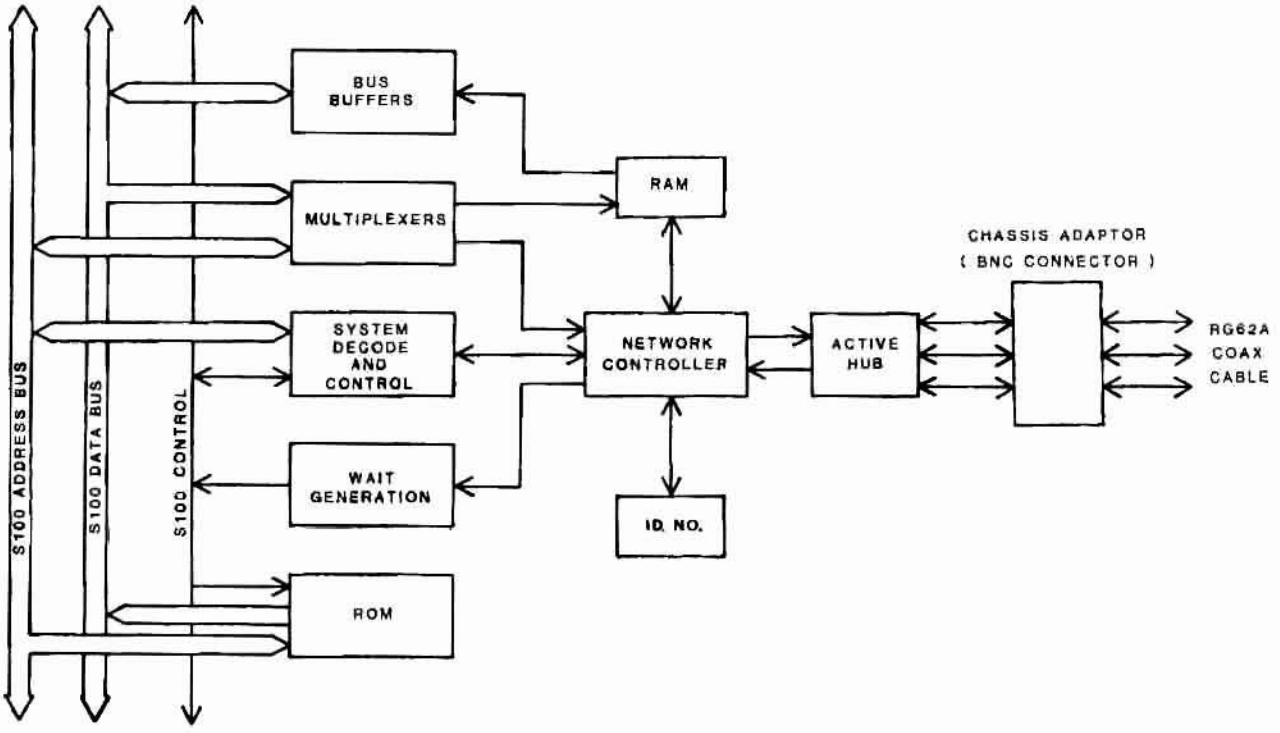


Figure 8-1. NET-100-1 Block Diagram

Theory of Operation

The NET-100-1 Card is divided into nine main sections.

- Bus Buffers
- Multiplexers
- System Decode and Control
- Wait Generation
- Read Only Memory (ROM)
- Random Access Memory (RAM)
- Network Controller
- ID Number
- Active Hub

The following paragraphs describe each of these sections.

Bus Buffers

The bus buffers are receivers and drivers for the S-100 address, data, and control signals.

Multiplexers (MUX)

The address/data multiplexers pass the 8-bit address onto the internal IAD0-IAD7 bus line to the network controller. The 8-bit data is then passed to the controller in the same way.

System Decode and Control

The system decode and control circuits contain all the logic necessary to control memory and I/O accesses, 8 and 16-bit data transfers, interrupts, and phantom assertion.

Wait Generation

The wait generation circuitry receives the network control wait signal and transforms it to the S-100 ready signal.

Read Only Memory (ROM)

The ROM allows the capability of booting in a non-disk environment. The support circuitry provides a 24-bit, switch selectable location in memory (phantom control optional through a jumper). The board does not come equipped with the ROM installed.

Random Access Memory (RAM)

The 2K × 8 RAM can be accessed by both the network controller and the system processor. The RAM location in memory is 24-bit, switch selectable on 2K boundaries.

Network Controller

The network controller provides the necessary interface between the S-100 Bus and the network. It controls waits, interrupts, and data to and from the system.

ID Number

The ID number is a unique number from 1 to 255 given to every node (unit) in the network. Physically set by an onboard switch, it serves to identify where a message is generated, where the message is being sent, and the priority that unit has.

Active Hub

The active hub decodes and encodes the incoming and outgoing messages. The hub allows implementation of a small network without any external hardware through the available three ports. The fourth port is dedicated to the network controller; no external connection may be made to it.

Chapter 9

Circuit Description

Introduction

This chapter provides a detailed circuit description of the NET-100-1 Card. Refer to the schematic diagrams for the following discussion.

Bus Buffers

U101, U102, U108, and U111 are the address bus buffers. U103 is the buffer for the data out (DO0-DO7) bus (data received from the S-100 Bus). U104 is a buffer for the data in (DI0-DI7) bus (data going out to the S-100 Bus). U104 is enabled by DBIN and REQ. U108 and U127 are buffers for the control signals.

Multiplexers

The multiplexers U112 and U118 select data transfers between the bus and the RAM or the network controller.

COM9026 Interface (U116)

First, output data to U116 through multiplexers U112 and U118 will be discussed. ADIE* (Address/Data Input Enable) from U116 pulses low, enabling the multiplexers through pin 15. Pin 1 on U112 and U118 are high since ILE* (Interface Latch Enable) is high. ILE* determines whether data or address bits are enabled onto the IAD0-IAD7 internal bus. While high, ILE* selects the B inputs (the address lines) of U112 and U118. After the address has been enabled to U116, ILE* and ADIE* pulse low, selecting the A inputs of U112 and U118, allowing U116 to latch the data on IAD0-IAD7.

An input access for data from U116 is very similar. The address is passed to U116 in the same manner as previously discussed. At this point, U116 outputs its data onto the IAD0-IAD7 bus. U104 then latches the data for output onto the DI0-DI7 S-100 Bus.

System Decode and Control

The memory access circuitry consists of U101, U105, U111, U134, SW101, and SW106. U105 and U134 are comparators which check the address on the bus, with the address set by SW101 and SW106. If the address checks, the outputs of U105-19 (MEMADRS2*) and U134-19 (MEMADRS1*) are low.

16-Bit Addressing

The I/O access circuitry consists of U110, U135, SW103, and SW107. When J105 pins 1 and 2 are jumpered together, the address on the bus is compared with the address set by SW107 and SW103. Listed below are the settings for I/O address switches selecting 00A0H. **Note that OFF equates to a logic "1" and ON to a logic "0".**

SW107

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A8	A9	A10	A11	A12	A13	A14	A15
ON/OFF	ON	ON	ON	ON	ON	ON	ON	ON

SW103

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A7	A6	A5	A4	A3	A2	A1	A0
ON/OFF	OFF	ON	OFF	ON	ON	ON	ON	ON

8-Bit Addressing

When J105 pins 2 and 3 are jumpered, only the address set by SW103 is compared. Although SW107 is not compared, the 8-bit addressing operates similarly to the 16-bit operation.

U107 is a 16L8 Programmable Array Logic (PAL). The PAL generates MREQ* (pin 13) and IOREQ* (pin 12) from IOADRS*, MEMADRS1* and MEMADRS2*, as shown by the PAL equations located in Chapter 12. MREQ* controls LED D105 through buffer U108. When active (low), the LED will light. LED D102 operates the same way, being controlled by IOREQ*. The S-100 Bus generates AS (Address Strobe) through U107, enabling U116 to sample MREQ* and IOREQ*.

Interrupt

One output from U107 is the INTR* line, U107-17. When U116 asserts its interrupt line (INTR 9026), U107 will force INTR* low, causing LED D103 to turn on after being buffered by U138. INTR* is connected to J101, a series of jumpers (refer to Figure 9-1). For use in the Z-100, VI2* is jumpered, although it is possible to jumper INT*, NMI* and VI0-VI7*. For the system to operate properly, only one jumper at a time can be used on J101.

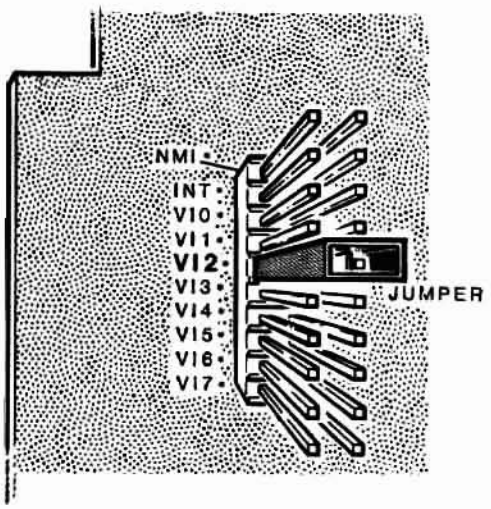


Figure 9-1. Interrupt Jumpers

Phantom

The other two outputs from U107, PHANTOM1* (pin 18) and PHANTOM2* (pin 15) are tied together. When MEMADRS1*, MEMADRS2* and a write cycle occur, PHANTOM2* goes low. In this way, the NET-100-1 board maps over ROM (Read Only Memory) space in the main system.

Wait Generation

At the beginning of every bus cycle (refer to Figure 9-2), the BSYNC pulse is fed to the preset lines (PR) pins 4 and 10 of flip-flop U139, forcing the Q output (pin 9) high and the Q* output (pin 8) low. The outputs remain in this state until the clock toggles the low in at U139-2.

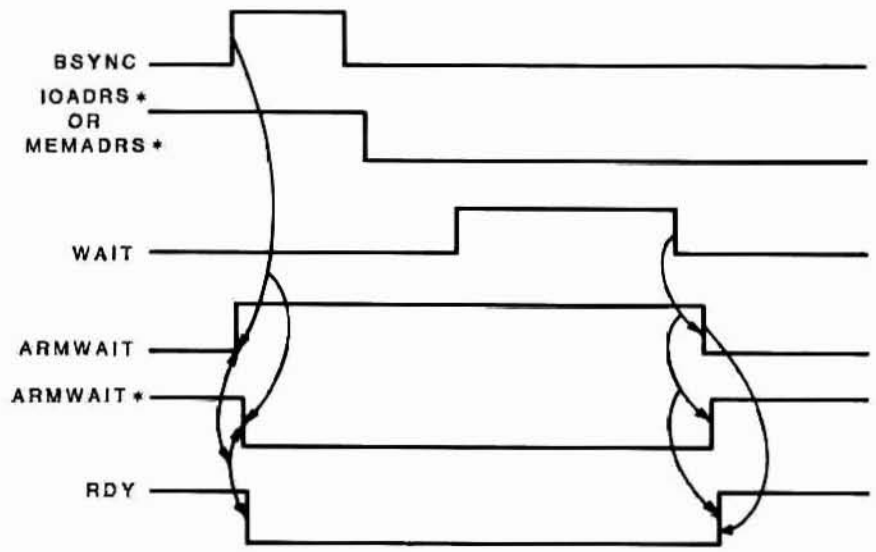


Figure 9-2. Timing Diagram

U139-8 (ARMWAIT*) is connected to U121-8. The other input of the NOR gate (U121-9) is IOADRS*. The output U121-10 is high if this board and I/O have been selected. When this occurs and bus status line BINP or BOUT (generated by U136-3) is high, U131-3 (RDY) is low, causing wait states to be inserted in that bus cycle until ARMWAIT* goes high.

U139-9 (ARMWAIT) is connected to U142-13. The other input to this gate is MEMADRS. When both MEMADRS1* and MEMADRS2* are low, U121-4 goes high, causing MEMADRS to be selected, and U142-11 to be high. U131-6 (RDY)is low if U142-11 and U131-4 (BINP or BOUT or BMEMR) are high.

In effect, when I/O or memory accesses occur on the NET-100-1 board, RDY is forced low. When U116 is ready, the WAIT signal becomes inactive, going low. WAIT is inverted at U133-11, clocking a low to the D input (pin 12) of U139. U139 is clocked by Φ*, synchronizing WAIT to the S-100 Bus timing. ARMWAIT goes low, forcing RDY high and ending the wait state.

ROM Circuitry

The ROM circuitry is independent from the network controller circuitry. It does not generate any wait states, nor does it rely on the wait states from the network controller to operate properly. After onboard buffering, the ROM circuitry operates as if it were a separate board within the unit.

U106, U108, U109, U130, U131, U133, U136, U140, SW102, and SW104 comprise the circuitry for the ROM (U117). U106 and U130 are comparators which check the address set by SW102 and SW104. When the address at SW102 is the same as that from the address bus, the output U106-19 goes low. U106-19 is connected to the input of U130. If both addresses check, ROMSEL* goes low, enabling the ROM via U117-20 (CE*).

The addresses A0-A12, required for U117, are taken from the buffered address bus. Depending on the memory type used, A13 may also be connected through J115, pins 1 and 2. Figure 9-3 illustrates the ROM insertion for the memory type used and Table 9-1 lists the jumper configuration for the selected ROM.

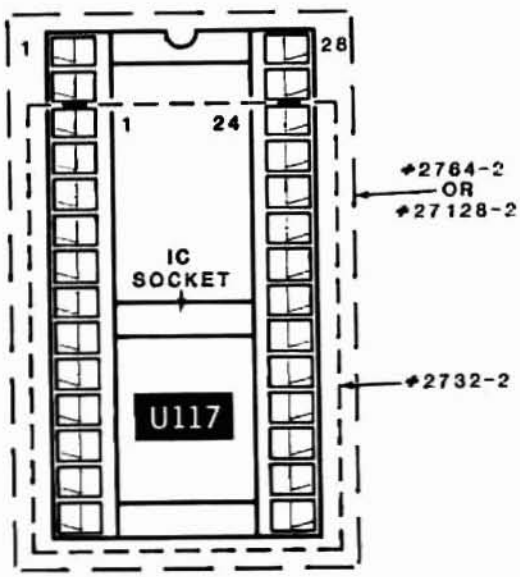


Figure 9-3. ROM Insertion

Table 9-1. ROM Jumper Configuration

TYPE	JUMPER	PINS JUMPERED
2732-2	J112	1,2
	J113	1,2
	J115	2,3
2764-2	J112	1,2
	J113	2,3
	J115	no jumper
27128-2	J112	2,3
	J113	2,3
	J115	1,2

The following switch settings of SW102 and SW104 correspond to address 0F4000H using a 2764 ROM:

SW102

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A16	A17	A18	A19	A20	A21	A22	A23
ON/OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON

SW104

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	NC	NC	NC	NC	NC	A15	A14	A13
ON/OFF	X	X	X	X	X	ON	OFF	ON

When a ROM read occurs from this board (DBIN and MEMR high), U133-3 (OE*) is low. OE* will enable the outputs (D0-D7) of U117 to U109. When U136 pins 9 (ROMSEL*) and 10 (OE*) are low, U109 pins 1 and 19 are low, allowing data to pass from the ROM to the DI0-DI7 of the S-100 Bus. A ROM read from this board results in ROMSEL and BMEMR being high, and the buffered output of U131, pin 11 being low, causing the LED D104 to light.

U131, an open collector NAND gate, is low when ROMSEL and MEMR go high. J114 is an optional jumper to allow this signal PHANTOM* to be asserted when the ROM is selected, allowing the ROM to be mapped over existing memory space. When configuring the Z-100, this jumper need not be used.

RAM Interface

U116 controls the timing for any RAM access, whether it is by the network controller or the system processor. When the address set by SW101 and SW106 equates with the address on the bus, the outputs of U105 (MEMADRS2*) and U134 (MEMADRS1*) go low. MEMADR1* and MEMADR2* outputs in coordination with the other inputs on the U107 (PAL) cause MREQ* to become active. The following switches are set to select 0F0000H, as used by the Z-100:

SW101

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A23	A22	A21	A20	A19	A18	A17	A16
ON/OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF

SW106

POSITION	0	1	2	3	4	5	6	7
ADDRESS BIT	A15	A14	A13	A12	A11	NC	NC	NC
ON/OFF	ON	ON	ON	ON	ON	X	X	X

After U116 receives MREQ*, it generates latch (L*), an active low pulse, enabling U122 to transfer the stable address on the internal IAD0-IAD7 bus to the RAM (U115). For a write cycle, U116 pulses ILE* low, enabling data to be multiplexed to the IAD0-IAD7 bus. WE* generated by U116 allows the latched data to be stored in U115. For a read cycle, the RAM sends data to the system processor or the network controller via the IAD0-IAD7 bus after U116 generates the OE* pulse to the RAM.

Network Controller

The network controller circuitry consists of U116, U123, and U124 (20 MHz oscillator). The network controller circuitry operates at a 2.5M bit data rate and works under a token passing scheme by passing an invitation to transmit to the next active ID number. U116 is the Local Area Network Controller (LANC) and U123 is the Local Area Network Transceiver (LANT). Together they provide the interface between the system and the network.

U124 provides the clock signal necessary for U123 to generate CA and CLK (pins 13 and 9) for U116 (pins 2 and 19). CLK is also used by U132 to clock the ID number to U116.

U123 also serves as an interface between the incoming/outgoing pulses on the interface modules (IM101 through IM103), and RX and TX* on U116. TX* (U116-37) is converted by U123 to PULS2*. Incoming signals (RXIN) are converted by U123 to RXOUT, which is connected to RX on the U116-38.

ID Number

When power or a keyboard reset is applied to the system, U116 reads the ID number from U132. The hardware is capable of selecting an ID number from 1 to 255, which is physically set by the user by SW105. The ID number is present at the parallel inputs of U132, pins 2, 3, 4, 5, 10, 11, 12, and 14. When U116 sends IDLD* (ID Load) and CLK to U132, the chip outputs the data in serial form, to U116-34, IDDAT (ID Data In). U116 stores the ID number in RAM location 01H. (The specific location in the Z-100 is F000:01H.)

The following switch setting designates ID number 100 (64H).

SW105

POSITION	0	1	2	3	4	5	6	7
ON/OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON

Active Hub

At initial power up of the system, U125-9 is momentarily held low by the RC network (R101 and C134) for 0.22 seconds. After being gated through U125, U141,and U142, this signal becomes PRSFF*. PRSFF* initializes the flip-flops (U120 and U129) so that the Q outputs are high and remain in that state until data from the network or this board pulses in a low at a D input.

Power up clears U119, initializing all of the Q outputs low. The Q outputs are the D inputs to U120 and U129 and remain low until a data pulse toggles one output high.

For example, assume the onboard port is the first to transmit. PULS2* from U123-1 is applied to U129-11 through inverter U140-4.
The low at U129-12 is clocked through to U119-13 (D4) and U128-3, putting a low (this will occur if any of the D inputs to U119 are low) at U142-3. This causes U125-11 to go high. U125-11 feeds four inputs: U137-12, U125-5, U128-9, and U128-2.

Remember that at this point, the Q outputs of U119 are still low, causing U141, pins 8, 10, and 12 to be high. These three high inputs to the AND gate (U128) cause the output to go high and provide U119 the required positive-edged clock. Q1, Q2,and Q3 of U119 remain high since the flip-flops have not toggled. The low at D4 is clocked through, causing Q4 to go low.

U137-9 (IDLE*) goes low 4.9 usec after a high is applied to U137-12. U137 is a one-shot whose timing is determined by R111 and C151.

IDLE* enables U127, which turns on the LED whose line is active. When no signal is present, U137-9 is high and the diodes (LED's) are unlit. In this case Q4 is low, therefore D109 will light. If one of the other ports is transmitting, the corresponding LED will light.

U137-10 is high at the same time as IDLE*, and causes U137-7 to go low after a time determined by R112 and C123 when IDLE becomes inactive (EOT). This signal is named EOT* and stands for End of Time. It is called this since a low on EOT* causes PRSFF* to reset the flip-flops in the same manner a power on of the system did.

U125-5 starts the pulse generation through the delay line (U126). The high on U125-5 is inverted and sent to U126-1. U126-12 (P1*) then goes low, and is connected to P1* of the interface modules. P2* goes low after P1*, and is connected to P2* of the interface modules. The interface modules generate the dipulse to the coax.

U126-6 goes low after the original input. U125 inverts the signal and U126-1, P1* and P2* go high, limiting their pulse widths to 100 nsecs. Note that P2* is inverted at U140-6 and connected to U123-10 (RXIN). U123 then generates RXOUT to U116. RXOUT is used for both U116 and the other three port network transmissions.

The Q outputs (either Q1, Q2, or Q3) of U119 are inverted by U141, and tied to the DIS/EN* lines (pin 19 of IM101-IM103). When the signal is high, the interface module is disabled and when low, it is enabled.

Initially, all the DIS/EN* lines are low, enabling the interface modules to receive data from the network. A high on the DIS/EN* line prevents the interface modules from retransmitting and disturbing any incoming data.

The hybrid interface modules provide interface to the coax cable (RG62). Pin 11 connects to the shield and 12 to the center of the coax cable. The shield is not tied to logic or chassis ground, but is AC coupled to chassis ground at the back panel through the chassis adapter box. Pins 6 and 3 of the interface modules are connected to +5V and −5V power supplies. Pin 7 (RX) is the incoming signal which is tied to the clock line on the flip-flops U120, pins 11 and 3, and U129, pin 3.

Chapter 10

Service Instructions

Introduction

This chapter contains information to assist in servicing and troubleshooting.

Check the jumpers and switches to be sure the NET-100-1 Card is configured properly. If these settings are all correct and the trouble is still present, refer to Table 10-1.

Troubleshooting

Table 10-1 lists some problems you may encounter and some possible causes.

Table 10-1. Troubleshooting

PROBLEM	POSSIBLE CAUSE
System fails to operate.	1. Be sure the card is fully seated in the card connector. 2. Be sure line cord is plugged in. 3. Check all jumpers. 4. Check all switches. 5. Inspect all I.C. packages for proper seating in sockets.
Card fails RAMTEST (LED D105)	1. Check SW101 and SW106 for correct selection. 2. Check MREQ* signal out of U107. If present U108, D105; otherwise U116, U111, U101, U134, U105, U107.
Card fails IOTEST (LED D102).	1. Check SW107 and SW103 for correct settings. 2. Check IOREQ* signal out of U107. If present U140, D102; otherwise U135, U110, U107.
Card fails MEMORY TEST.	1. U102, U103, U104, U112, U118, U122, U132, U138, U115.
Interrupt LED D103 does not light when INTR* is asserted.	1. U138, D103.

(Continued...)

Service Instructions

Table 10-1. Troubleshooting (continued...)

PROBLEM	POSSIBLE CAUSE
ROM LED D104 does not light when ROM is being mapped.	1 Check for correct settings on SW102 and SW104. 2. Check ROMSEL* signal out of U130. If present U140, U131, D104; otherwise U106, U130.
ROM inoperative.	1. U108, U133, U136, U109, U117.
RDY signal not generated.	1. U133, U139, U121, U136, U140, U142, U131, U116.
All ports inoperable.	1. U116, U123, U124, U125, U142, U129, U119, U128, U141, U126.
Ports 1, 2, and 3 inoperable.	1. U111, U119, U137.
Onboard port inoperable. (LED D109 not lit)	1. U123, U140, U129, U128, U119, U127, D109.
Port 3 inoperable. (LED D108 not lit)	1. Bad coax. IM103, U141, U120, U128, U119, U127, D108.
Port 2 inoperable. (LED D107 not lit)	1. Bad coax. IM102, U141, U129, U128, U119, U127, D107.
Port 1 inoperable. (LED D106 not lit)	1. Bad coax. IM101, U141, U119, U27, D106.
EMI emissions	1. Bad ground between network interface and S-100.

Chapter 11

Parts List

Introduction

This chapter includes a component view of the NET-100-1 Card and an exploded view of the Network Chassis Adapter to assist in the identification for replacement parts. Adjacent to the circuit reference designator or exploded view number are the part number and description which must be supplied when ordering a replacement part.

Replacement Parts

NET-100-1 Network Card

The NET-100-1 Card is Part Number 181-4638-1. Refer to Figure 11-1 to identify replacement parts.

CAUTION: This board contains ESDS (Electrostatic Sensitive devices). Exercise extreme care in handling these devices to prevent damage.

NOTE: Refer to the Semiconductor Identification section of this chapter, or Chapter 12, Data Sheets, for description of semiconductor devices.

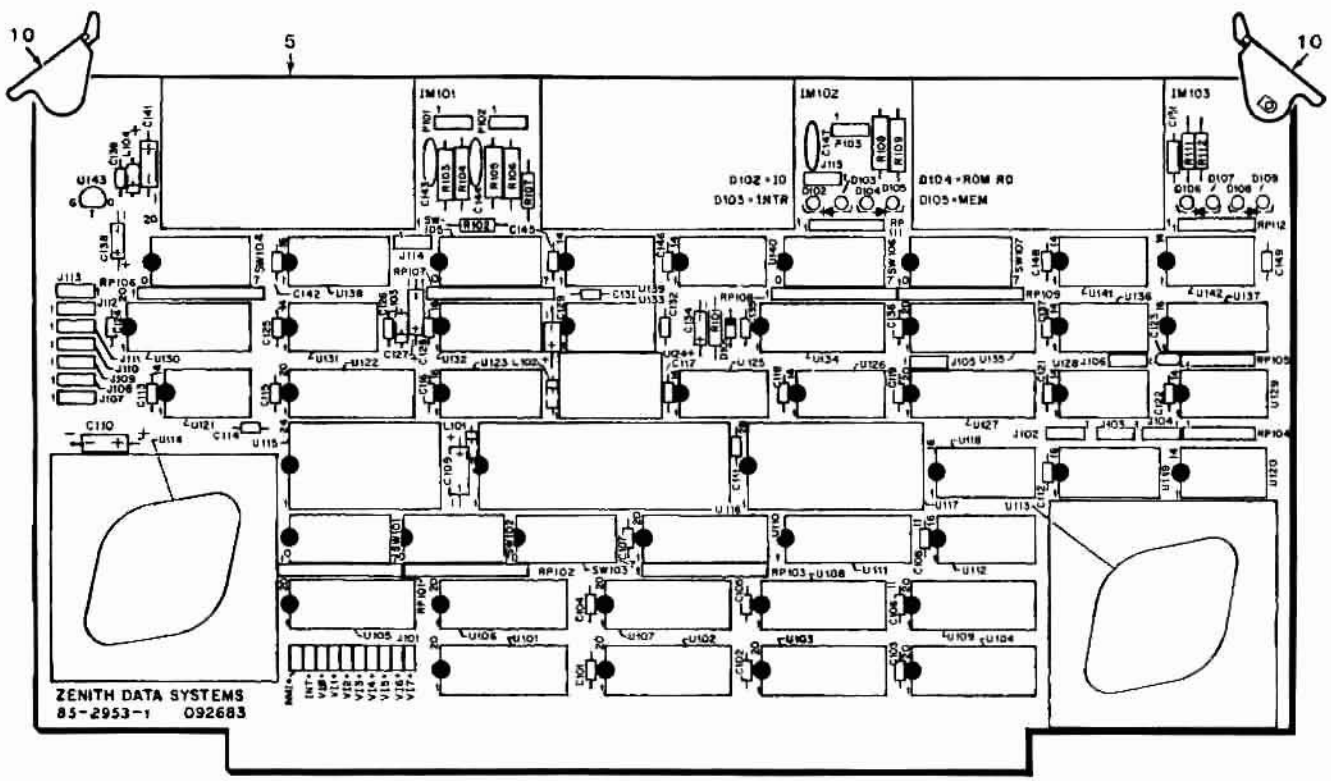


Figure 11-1. Component View NET 100-1 Card

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors		
C101	HE 21-769	.01 µF ceramic
C102	HE 21-769	.01 µF ceramic
C103	HE 21-769	.01 µF ceramic
C104	HE 21-769	.01 µF ceramic
C105	HE 21-769	.01 µF ceramic
C106	HE 21-769	.01 µF ceramic
C107	HE 21-769	.01 µF ceramic
C108	HE 21-769	.01 µF ceramic
C109	HE 25-195	2.2 µF tantalum
C110	HE 25-195	2.2 µF tantalum
C111	HE 21-769	.01 µF ceramic
C112	HE 21-769	.01 µF ceramic
C113	HE 21-769	.01 µF ceramic
C114	HE 21-769	.01 µF ceramic
C115	HE 21-769	.01 µF ceramic
C116	HE 21-769	.01 µF ceramic
C117	HE 21-769	.01 µF ceramic
C118	HE 21-769	.01 µF ceramic
C119	HE 21-769	.01 µF ceramic
C120	Not Used	
C121	HE 21-769	.01 µF ceramic
C122	HE 21-769	.01 µF ceramic
C123	HE 21-750	56 pF ceramic
C124	HE 21-769	.01 µF ceramic
C125	HE 21-769	.01 µF ceramic
C126	HE 21-769	.01 µF ceramic
C127	HE 25-195	2.2 µF tantalum
C128	HE 21-769	.01 µF ceramic
C129	HE 25-195	2.2 µF tantalum
C130	Not Used	
C131	HE 21-769	.01 µF ceramic
C132	HE 21-769	.01 µF ceramic
C133	Not Used	
C134	HE 25-962	4.7 µF tantalum
C135	HE 21-769	.01 µF ceramic
C136	HE 21-769	.01 µF ceramic
C137	HE 21-769	.01 µF ceramic
C138	HE 25-962	4.7 µF tantalum
C139	HE 21-769	.01 µF ceramic
C140	Not Used	
C141	HE 25-195	2.2 µF tantalum
C142	HE 21-769	.01 µF ceramic
C143	Not Used	
C144	Not Used	
C145	HE 21-769	.01 µF ceramic
C146	HE 21-769	.01 µF ceramic
C147	Not Used	
C148	HE 21-769	.01 µF ceramic
C149	HE 21-769	.01 µF ceramic
C150	Not Used	
C151	HE 21-173	2200 pF ceramic
Diodes		
D101	HE 56-56	1N4149
D102	HE 412-654	LED, red
D103	HE 412-654	LED, red
D104	HE 412-654	LED, red
D105	HE 412-654	LED, red
D106	HE 412-654	LED, red
D107	HE 412-654	LED, red
D108	HE 412-654	LED, red
D109	HE 412-654	LED, red
Interfaces and Jumpers		
IM101	HE 234-425	Cable interface
IM102	HE 234-425	Cable interface
IM103	HE 234-425	Cable interface
J101	HE 432-1073	Pin 10M MOLEX
	HE 432-1041	Pin 2F BERG
J102	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG
J103	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG
J104	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG
J105	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG
J106	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
J107	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG
J108	HE 432-1041	Pin 2F BERG
	HE 432-1102	Pin 3M MOLEX
J109	HE 432-1041	Pin 2F BERG
	HE 432-1102	Pin 3M MOLEX
J110	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG
J111	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG
J112	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG
J113	HE 432-1102	Pin 3M MOLEX
	HE 432-1041	Pin 2F BERG
J114	HE 432-1102	Pin 3M MOLEX
Chokes and Pins		
L101	HE 235-229	35uh RF choke
L102	HE 235-229	35uh RF choke
L103	HE 235-229	35uh RF choke
L104	HE 235-229	35uh RF choke
P101	HE 432-986	Pin 3M MOLEX right angle
P102	HE 432-986	Pin 3M MOLEX right angle
P103	HE 432-986	Pin 3M MOLEX right angle
Resistors		
R101	HE 6-4532-12	45.3 kohm
R102	HE 6-102-12	1 kohm
R103	HE 6-562	5.6 kohm
R104	HE 6-562	5.6 kohm
R105	HE 6-562	5.6 kohm
R106	HE 6-562	5.6 kohm
R107	HE 6-102-12	1 kohm
R108	HE 6-562	5.6 kohm
R109	HE 6-562	5.6 kohm
R110	Not Used	
R111	HE 6-103-12	10 kohm
R112	HE 6-512-12	5.1 kohm
RP101	HE 9-128	10 kohm resistor pack
RP102	HE 9-128	10 kohm resistor pack
RP103	HE 9-128	10 kohm resistor pack
RP104	HE 9-99	1 kohm resistor pack
RP105	HE 9-99	1 kohm resistor pack
RP106	HE 9-128	10 kohm resistor pack
RP107	HE 9-128	10 kohm resistor pack
RP108	HE 9-128	10 kohm resistor pack
RP109	HE 9-128	10 kohm resistor pack
RP110	Not Used	
RP111	HE 9-120	150 ohm resistor pack
RP112	HE 9-120	150 ohm resistor pack
Switches		
SW101	HE 60-657	DIP, SPST
SW102	HE 60-657	DIP, SPST
SW103	HE 60-657	DIP, SPST
SW104	HE 60-657	DIP, SPST
SW105	HE 60-657	DIP, SPST
SW106	HE 60-657	DIP, SPST
SW107	HE 60-657	DIP, SPST
Semiconductors		
U101	HE 443-980	Driver
	HE 434-311	Socket
U102	HE 443-791	Buffer/driver tri-state
	HE 434-311	Socket
U103	HE 443-791	Buffer/driver tri-state
	HE 434-311	Socket
U104	HE 443-837	Latch 8-bit tri-state
	HE 434-311	Socket
U105	HE 443-1159	8-bit comparator
	HE 434-311	Socket
U106	HE 443-1159	8-bit comparator
	HE 434-311	Socket
U107	HE 444-222	PAL S-100/9026 timing
	HE 434-311	Socket
U108	HE 443-980	Driver
	HE 434-311	Socket
U109	HE 443-791	Buffer/driver tri-state
	HE 434-311	Socket
U110	HE 443-1159	8-bit comparator
	HE 434-311	Socket

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
U111	HE 443-980	Driver
	HE 434-311	Socket
U112	HE 443-802	MUX quad 2 input tri-state
	or	
	HE 443-1178	
	HE 434-299	Socket
U113	HE 442-702	Voltage regulator
	HE 215-675	Heat sink
	HE 250-1429	Screw 6-32 × .375"
	HE 254-1	Washer #6 lock
	HE 252-77	Nut 6-32 × .250"
U114	HE 442-702	Voltage regulator
	HE 215-675	Heat sink
	HE 250-1429	Screw 6-32 × .375"
	HE 254-1	Washer #6 lock
	HE 252-77	Nut 6-32 × .250"
U115	HE 443-1027	RAM 2k × 8
	HE 434-307	Socket
U116	HE 443-1161	LANC controller
	HE 434-253	Socket
U117	Not Supplied	
	HE 434-312	Socket
U118	HE 443-802	MUX quad 2 input tri-state
	or	
	HE 443-1178	
	HE 434-299	Socket
U119	HE 443-752	Quad D F-F
	HE 434-299	Socket
U120	HE 443-900	Dual D F-F
	HE 434-298	Socket
U121	HE 443-896	Quad NOR 2 input
	HE 434-298	Socket
U122	HE 443-837	Latch 8-bit tri-state
	HE 434-311	Socket
U123	HE 443-1162	LANT transciever
	HE 434-298	Socket
U124	HE 150-162	Crystal oscillator
U125	HE 443-26	Quad NAND 2 input
	HE 434-298	Socket
U126	HE 41-18	Delay line
	HE 434-298	Socket
U127	HE 443-791	Buffer/driver tri-state
	HE 434-311	Socket
U128	HE 443-1046	Triple AND 3 input
	HE 434-298	Socket
U129	HE 443-900	Dual D F-F
	HE 434-298	Socket
U130	HE 443-1159	8-bit comparator
	HE 434-311	Socket
U131	HE 443-1128	NAND 2 input open collector
	HE 434-298	Socket
U132	HE 443-892	Register
	HE 434-299	Socket
U133	HE 443-26	Quad NAND 2 input
	HE 434-298	Socket
U134	HE 443-1159	8-bit comparator
	HE 434-311	Socket
U135	HE 443-1159	8-bit comparator
	HE 434-311	Socket
U136	HE 443-1133	Quad 2 input OR gate
	HE 434-298	Socket
U137	HE 443-1112	D/ retrg mon multvbrt
	HE 434-299	Socket
U138	HE 443-857	Buffer hex tristate
	HE 434-299	Socket
U139	HE 443-900	Dual D F-F
	HE 434-298	Socket
U140	HE 443-897	Hex inverter
	HE 434-298	Socket
U141	HE 443-897	Hex inverter
	HE 434-298	Socket
U142	HE 443-976	Quad AND 2 input
	HE 434-299	Socket
U143	HE 442-665	−5V regulator

ITEM NUMBER	PART NUMBER	DESCRIPTION
5	85-2940-1	PC board
10	266-1203	Circuit board extenders

Parts List

Network Chassis Adapter

Network Chassis Adapter is Part Number 191-3637-1. Refer to Figure 11-2.

ITEM NUMBER	PART NUMBER	DESCRIPTION

ITEM NUMBER	PART NUMBER	DESCRIPTION

ITEM NUMBER	PART NUMBER	DESCRIPTION
5	200-1466-1	Chassis with BNC adaptors
10	250-1434	Screw 6-BT × .375"
15	259-27	Solder lug
20	344-222	Red wire
25	432-866 or 432-1063	1 MOLEX
30	432-865	3F MOLEX
35	344-220	Black wire
40	21-46	5000 pf capacitor
45	259-1	Solder lug
60	253-746	Washer, insulated

Parts List

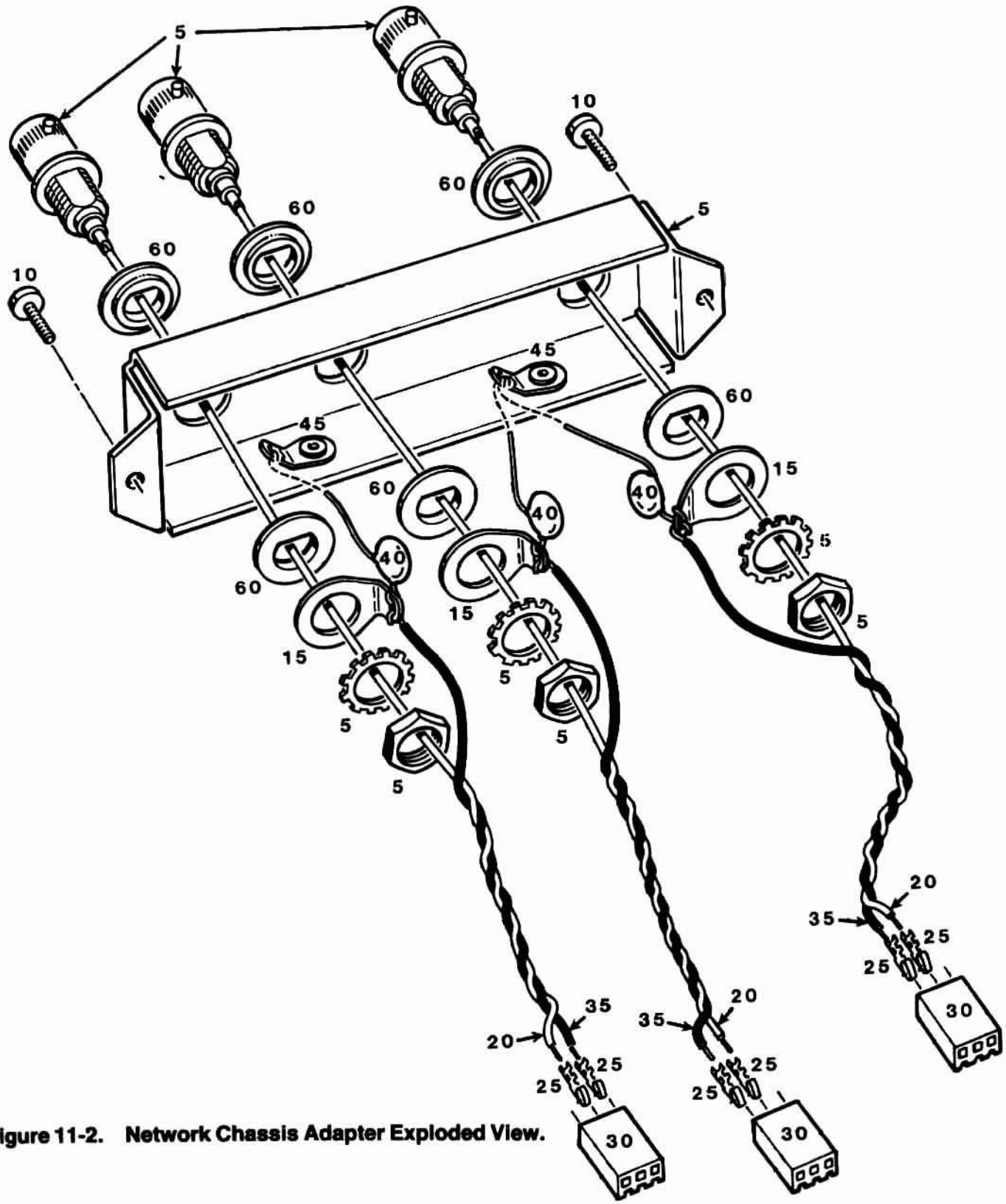


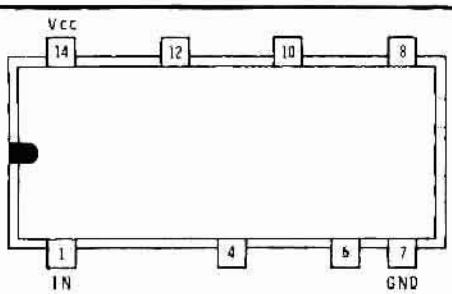
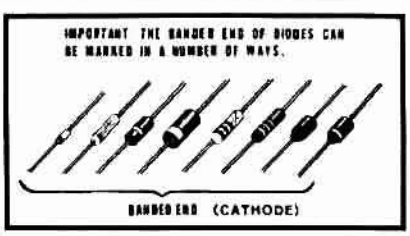
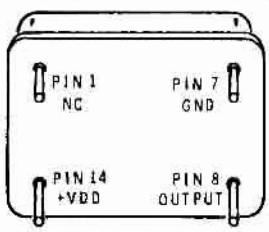
Figure 11-2. Network Chassis Adapter Exploded View.

Parts List

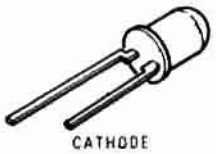
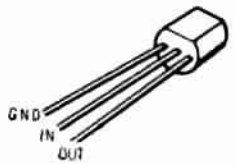
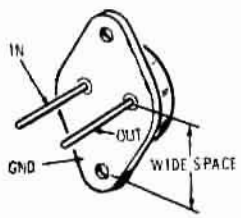
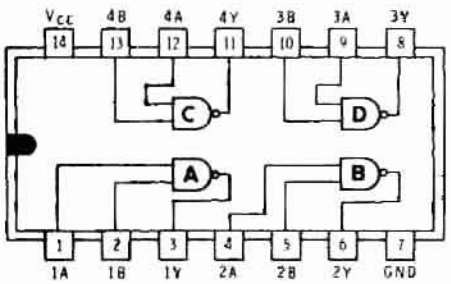
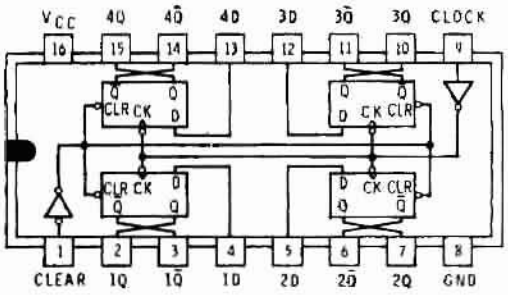
Semiconductor Identification

This section provides assistance in semiconductor identification by use of a cross reference between Heath part numbers and semiconductor part numbers. The Heath part numbers are listed in numerical order with replacement part numbers (if available), description, and lead configuration in adjacent columns. The PAL equations also are presented in this chapter.

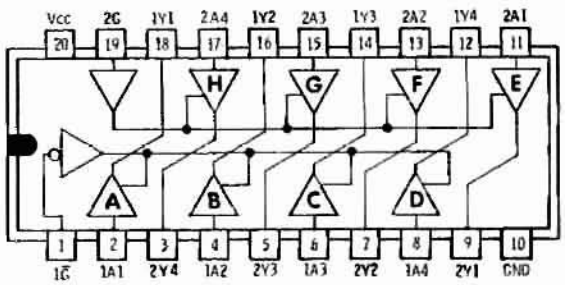
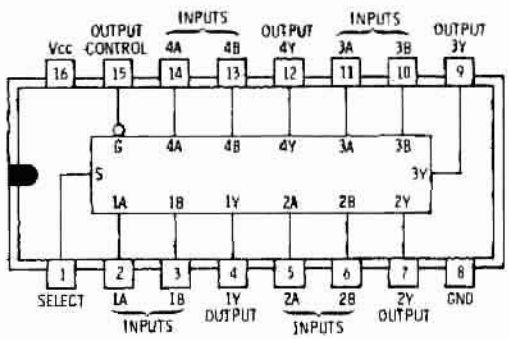
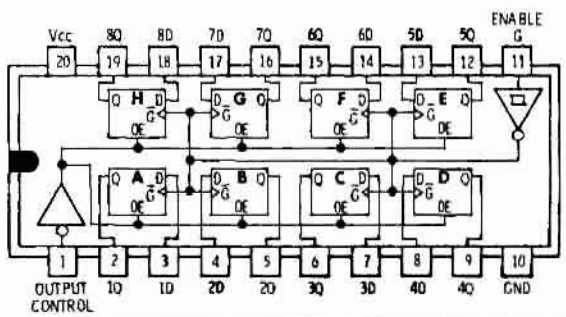
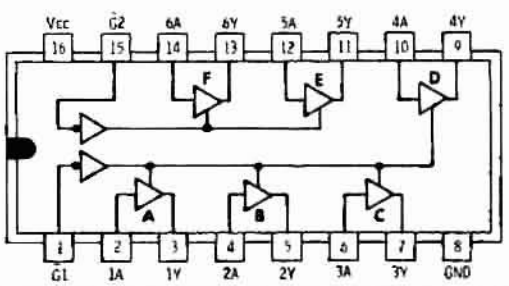
Part Number Index

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
41-18	DL-14CB125	U126 125ns delay line	
56-56	1N4149	D101 Diode	
150-162	Available only from Zenith Data Systems or Heath Company	U124 20 MHZ crystal oscillator	

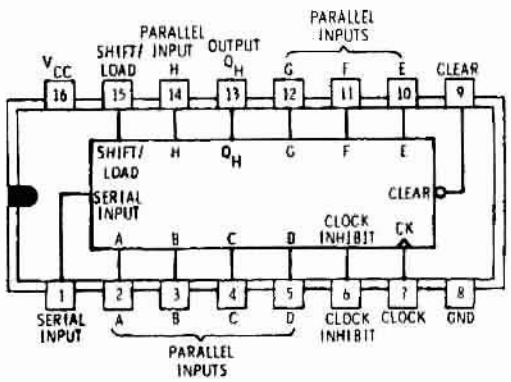
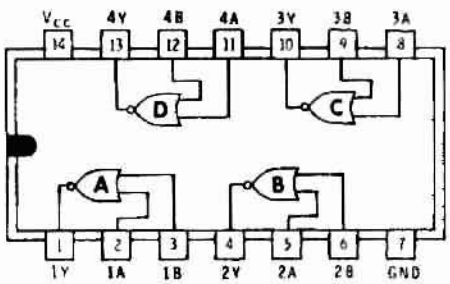
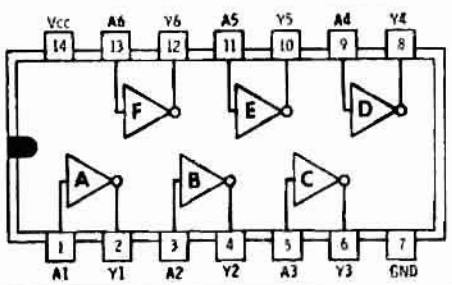
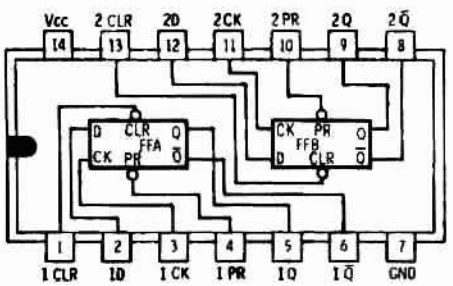
Parts List

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
412-654	Available only from Zenith Data Systems or Heath Company	D102 through D109 Light Emitting Diode (LED)	
442-665	79L05	U143 – 5V Voltage regulator	
442-702	LM323	U113, U114 + 5V Voltage regulator	
443-26	74S00	U125, U133 Quad 2-input NAND	
443-752	74LS175	U119 Quad D-type flip-flop	

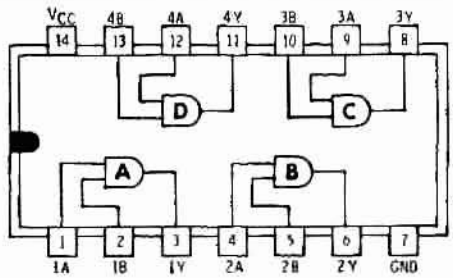
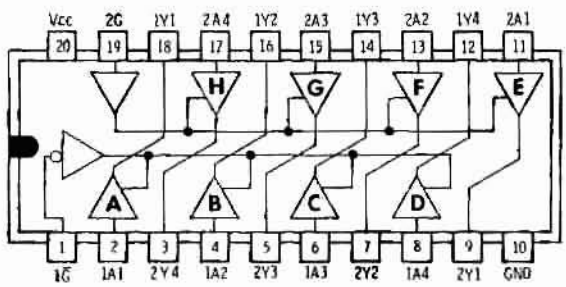
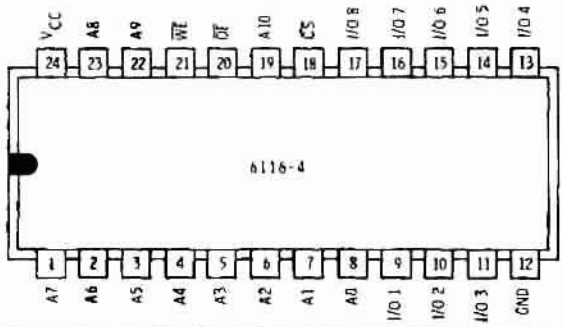
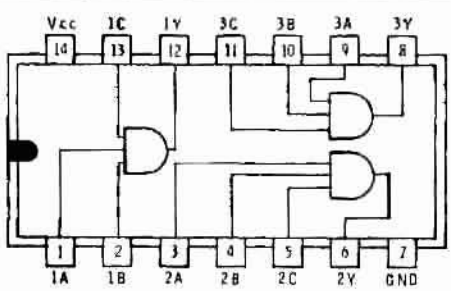
Parts List

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-791	74LS244	U102, U103, U109, U127 Noninverting 3-state output octal buffers	
443-802 or 443-1178	74LS257 or 74ALS257	U112, U118 Quad 2-input 3-state multiplexer	
443-837	74LS373	U104, U122 3-state 8-bit latch	
443-857	74LS367	U138 Hex bus driver	

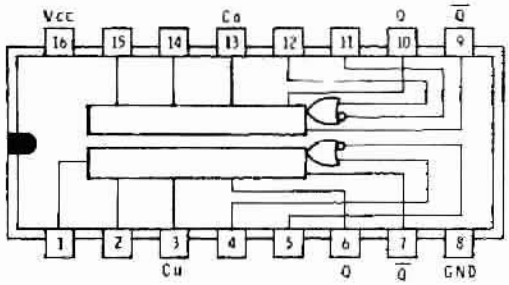
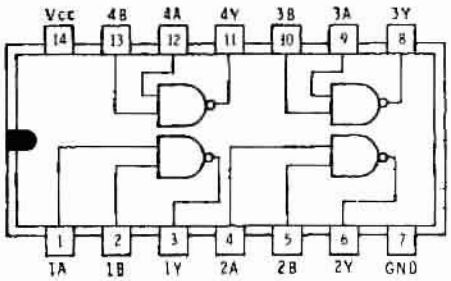
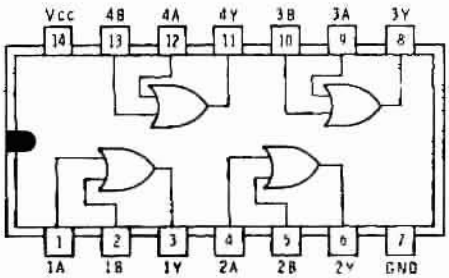
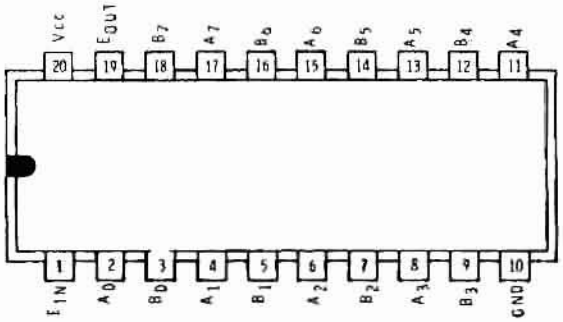
Parts List

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-892	74LS166	U132 Register	
443-896	74S02	U121 Quad 2-input NOR	
443-897	74S04	U140, U141 HEX inverter	
443-900	74S74	U120, U129 Dual D flip-flop	

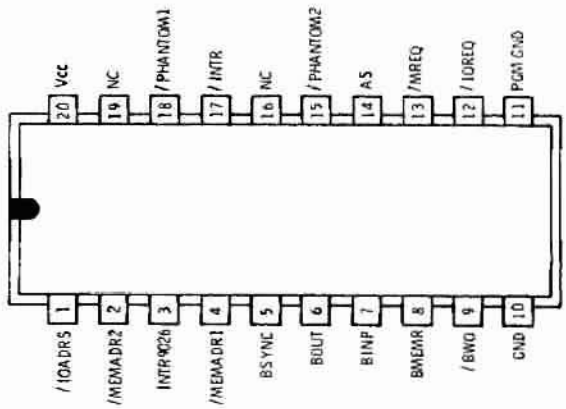
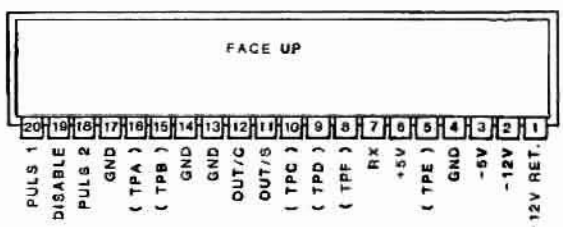
Parts List

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-976	74S08	U142 Quad 2-input AND	
443-980	74S244	U101, U108, U111 Noninverting 3-state output octal buffers	
443-1027	6116-P4	U115 2K × 8 RAM	
443-1046	74S11	U128 Triple 3-input AND	

Parts List

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
443-1112	9602	U137 D retriggerable monostable multivibrator	
443-1128	74S03	U131 Open collector 2-input NAND	
443-1133	74S32	U136 Quad 2-input OR	
443-1159	25LS2521	U105, U106, U110, U130, U134, U135 8-bit comparator	

Parts List

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
444-222	Available only from Zenith Data Systems or Heath Company	U107 PAL16L8 memory timing control	
234-425	Available only from Zenith Data Systems or Heath Company	IM101 IM102 IM103 Cable Interface	

PAL Equations

PAL equations are Boolean expressions where / equals a negated signal, * equals an AND function, and + equals an OR function.

PAL16L8
444-222
S-100 Bus/9026 Interface

/IOADRS, /MEMADR2, INTR9026, /MEMADR1, BSYNC, BOUT, BINP, BMEMR, /BWO, GND, PGMGND, /IOREQ, /MREQ, AS, /PHANTOM2, NC, /INTR, /PHANTOM1, NC, VCC

IF (MEMADR2 * MEMADR1 * /BOUT * BWO) PHANTOM2 = PGMGND

IF (INTR9026) INTR = INTR9026

IF (MEMADR2 * MEMADR1 *BMEMR) PHANTOM1 = PGMGND

/AS = /BSYNC

MREQ = MEMADR2 * MEMADR1 * MEMR + MEMADR2 * MEMADR1 * /BOUT * BWO IOREQ = IOADRS * BINP + IOADRS * BOUT

Chapter 12

Data Sheets

Introduction

This chapter contains the the necessary technical information to understand the COM 9026, Local Area Network Controller (LANC), and the COM 9032, Local Area Network Transceiver (LANT). The following pages are reprinted with the permission of Standard Microsystems Corporation.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510 227-8898

TECHNICAL NOTE TN5-2

USING THE COM 9026 LOCAL AREA NETWORK CONTROLLER AND THE COM 9032 LOCAL AREA NETWORK TRANSCEIVER

The purpose of this technical note is to provide the information and schematics needed to implement the CLOCK GENERATOR and the CABLE TRANSCEIVER for the COM 9026. In addition, some discussion of the transmission media network topology and network performance is included.

CLOCK GENERATOR

Figures 1 and 2 illustrate the CLOCK GENERATOR and associated timing respectively. The purpose of this circuitry is to generate the CLK and CA signals for the COM 9026. A 20 MHz oscillator is used to allow proper control of the starting and stopping of the CA signal. The CLK signal is generated from a divide by 4 circuit using 2 74S112's.

The line protocol of the COM 9026 is designed to ensure that a negative transition always occurs 1 bit time before a particular byte of any transmission. A three bit field of 110, which proceeds every byte, provides the required negative transition. The "0" in this three bit field may be thought of as a start bit and the "11" may be thought of as two stop bits from the previous byte. When the COM 9026 is waiting for another byte (or the first byte) within a message, it will resynchronize the CA clock by temporarily halting the CA clock at the high level. It accomplishes this by lowering the $\overline{\text{DSYNC}}$ signal. When the RX line experiences a high to low transition (the "0" in the three bit field), the CA clock is restarted which in turn causes the $\overline{\text{DSYNC}}$ signal to be raised to the high level. The circuitry of figure 1 assumes an RX bit spacing of 400 nanoseconds which must be equal to twice the period of the CA clock. The circuitry of figure 1 is set up such that the next low to high transition of the CA clock occurs between 200 and 250 nanoseconds after the high to low transition on RX. This places the point at which the COM 9026 samples the RX input approximately midway into the bit. Every other low to high transition on CA thereafter will be used to sample the 8 bit data byte that follows. Once the byte is received, the $\overline{\text{DSYNC}}$ signal is again activated in preparation for the next high to low transition on the RX line indicating the start of the next data byte. The $\overline{\text{DSYNC}}$ output will return to its high (inactive) state after each CA synchronization is established. Figure 3 illustrates the relationship of the $\overline{\text{DSYNC}}$, CA and RX signals before, during, and after CA synchronization.

The technique used for synchronization is similar to that of standard asynchronous protocols where a sample point within an asynchronous signal is found and used for each byte transmitted. Traditionally, a 16X or 64X clock is used to provide the resolution needed to find the proper sample point for low frequency transmission. Because of the 2.5 M bit rate provided by the COM 9026, a 2X clock (the CA signal) is used in conjunction with an external 8X clock (20 MHz) to allow determination of a reliable sample point.

It should be noted that the $\overline{\text{DSYNC}}$ output can never become active low during a COM 9026 transmission. At the end of a transmission, the COM 9026 will wait about 6 microseconds. By this time the line should be quiet and the RX input will be sitting in a space (low) condition. At this time, the COM 9026 will wait for the RX input to become high (level sensitive not edge sensitive) which occurs during the alert burst of the next transmission. At this time, the COM 9026 starts reception by lowering the $\overline{\text{DSYNC}}$ signal.

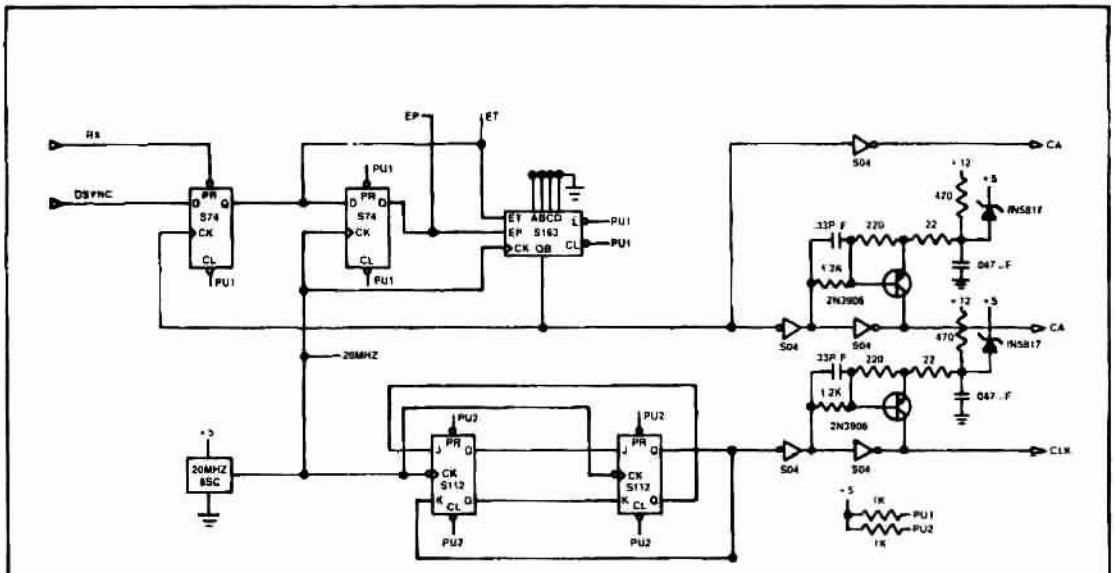


FIGURE 1: CLOCK GENERATION*

*Suggested circuit when using the COM9026 without the COM9032

Data Sheets

CABLE TRANSCEIVER

The circuitry of figure 1 and the COM 9026 assume the data appearing on the RX signal is NRZ with a high level indicating a logic "1" and a low level indicating a logic "0". The bit boundaries are spaced at 400 nanosecond intervals, establishing the 2.5 M bit data rate. The COM 9026, when transmitting data on $\overline{TX}$, will produce a negative pulse of 200 nanoseconds in duration to indicate a logic "1" and no pulse to indicate a logic "0". Figure 5 illustrates a typical data transmission.

The CABLE TRANSCEIVER's function is first to convert the 200 nanosecond $\overline{TX}$ pulses output by the COM 9026 to a format consistant with the transmission media and network topology and, second, to convert signals from the cable to the NRZ data required by the COM 9026's RX input. Starting with the $\overline{TX}$ and RX signals, many different cable transceiver implementations can result to allow for broadband or baseband networks using twisted pair, coax, or fiber optics as the transmission media. Figures 4 and 6 illustrate a typical CABLE TRANSCEIVER used to implement Datapoint's ARCNET* local area network. The ARCNET* implementation uses a baseband system with RG62 (93 ohm) coax.

Referring to figure 4, a 200 nanosecond negative pulse on $\overline{TX}$ is converted to two 100 nanosecond negative pulses shown as $\overline{PULSE\ 1}$ and $\overline{PULSE\ 2}$. These two signals are used to create a 200 nanosecond wide dipulse signal by being driven into opposite sides of RF transformer T1 and finally coupled onto the coax as shown in figure 6. Figure 7 shows the timing relationship between CA, $\overline{TX}$, $\overline{PULSE\ 1}$ and $\overline{PULSE\ 2}$. The waveform of the resultant dipulse is also shown in figure 7.

Referring to figure 6, a dipulse appearing on the coax is coupled to the receiver via RF transformer T1 and passed through a filter network matched to the 93 ohm characteristic impedance of the coax. The filter output feeds a 75108 comparator which produces a positive pulse on RCVD for each dipulse received from the coax. The RCVD signal feeds the circuitry shown in figure 4 which converts these pulses to NRZ data on the RX signal entering the COM 9026. Figure 8 illustrates the timing associated with this function.

The CABLE TRANSCEIVER shown in figures 4 and 6 has been designed to operate in a baseband cable system using a network topology where any 2 nodes are connected by a single path which is terminated at both ends with the cable's characteristic impedance. Figure 9 illustrates a typical free forming tree topology which is used in the ARCNET* implementation. By using central HUBs, each node connects through a length of cable to a port on a HUB with the cable terminated as previously described. No taps are used on the coax.

The COM 9032 local area network transceiver, housed in a 16 pin package, can replace all the logic shown in figures 1 and 4 and simplify the building of ARCNET* compatible networks by performing the following functions;

1- Generation of CA and CLK clocks for the COM 9026 with high voltage drive.
2- Creation of $\overline{PULSE\ 1}$ and $\overline{PULSE\ 2}$ waveforms during transmit.
3- Conversion of received data to NRZ format.

These functions are performed exactly as the TTL implementation shown in figures 1 and 4. Figure 10 illustrates the COM 9032 used with the COM 9026 to implement an ARCNET* compatible cable transceiver.

*ARCNET is a registered trademark of the Datapoint Corporation

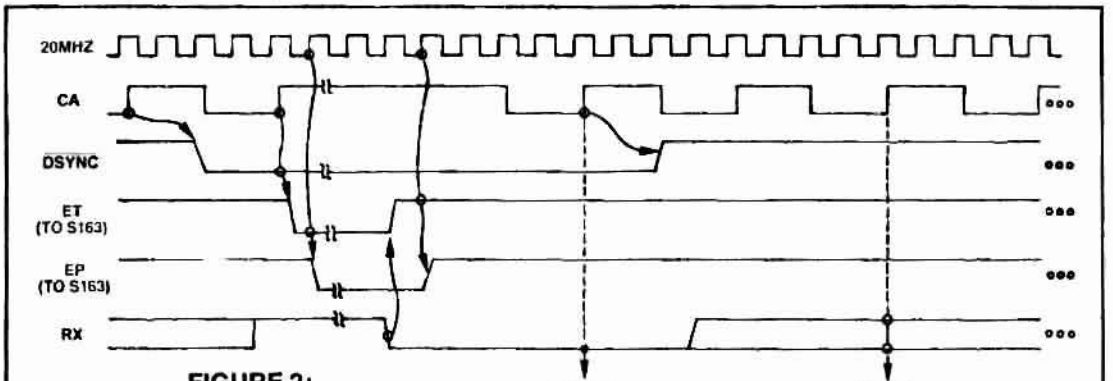


FIGURE 2: RECEIVE SYNCHRONIZATION TIMING

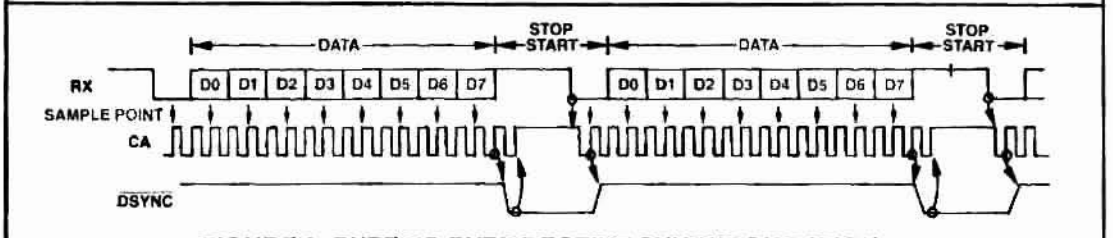


FIGURE 3: BYTE TO BYTE RECEIVE SYNCHRONIZATION

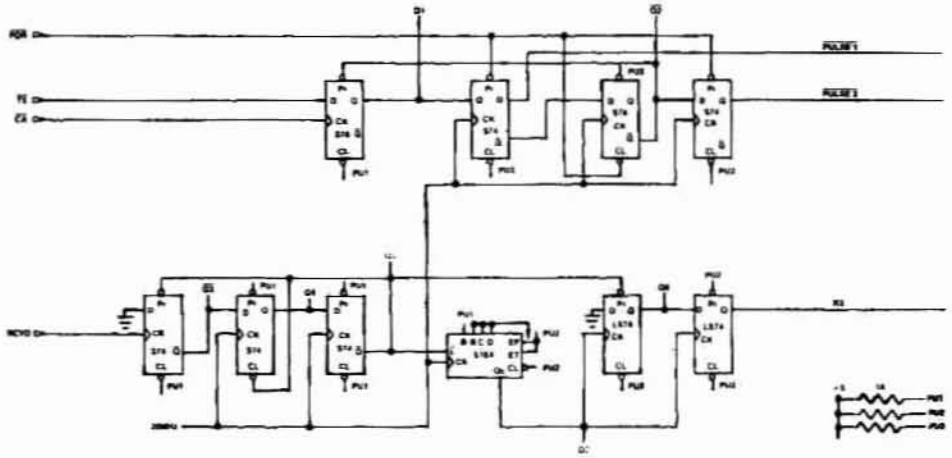


FIGURE 4: TRANSMIT AND RECEIVE LOGIC*

*Suggested circuit when using the COM9026 without the COM9032.

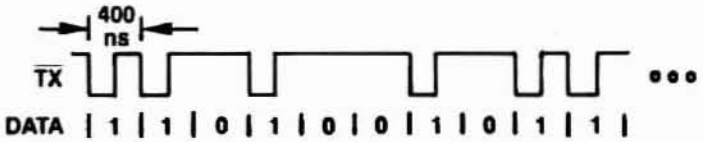


FIGURE 5: TYPICAL $\overline{TX}$ WAVEFORM

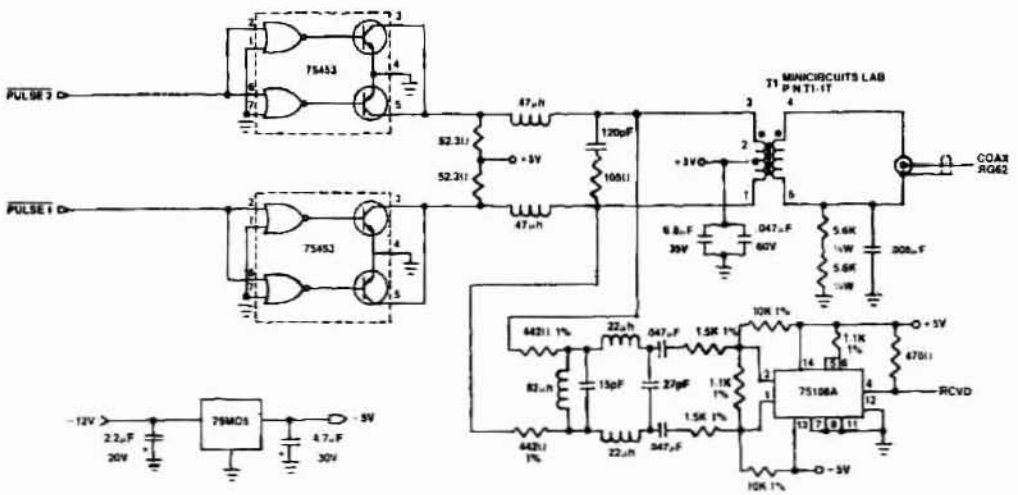


FIGURE 6: ARCNET* CABLE TRANSCEIVER

*ARCNET is a registered trademark of the Datapoint Corporation

Data Sheets

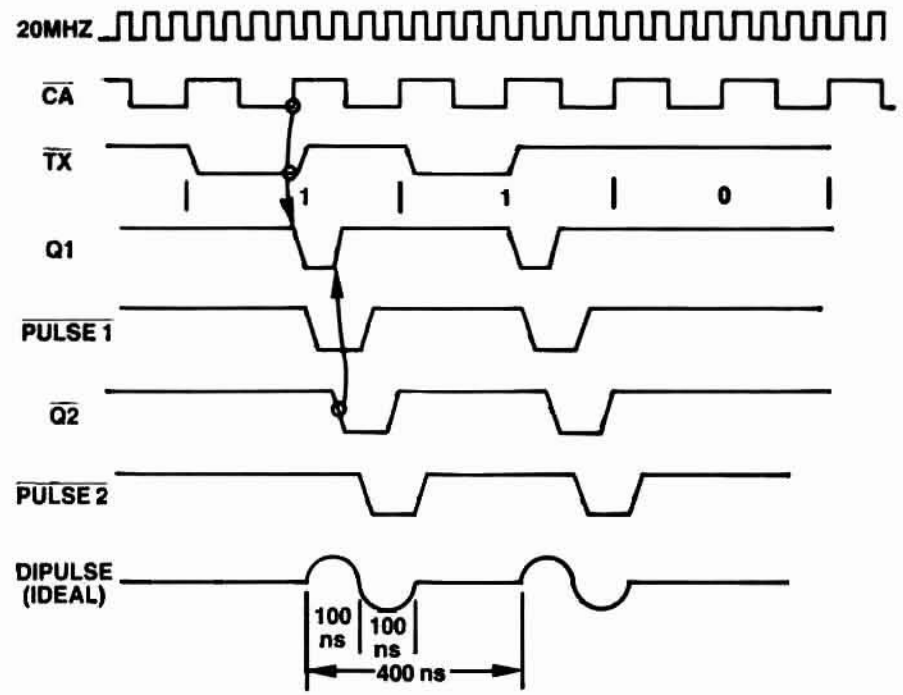


FIGURE 7: DIPULSE GENERATION

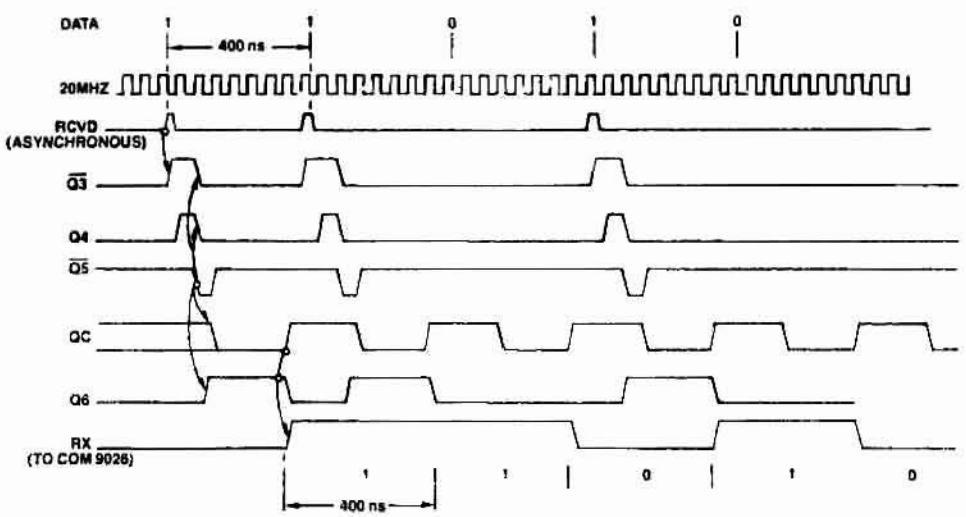


FIGURE 8: RX WAVEFORM GENERATION

HUB ELECTRONICS

Figures 11a and 11b illustrate a typical implementation of an active HUB. The HUB may be thought of as an amplifier and a number of ideal taps mounted in the same box. Each tap is ideal in that it causes no insertion loss, no tap loss and provides total suppression of reflections. Each of the ports on the HUB may be connected to a network node, to another HUB, to an unterminated length of coax, or to nothing at all. The reflections caused by connecting an unterminated length of coax is taken into account in the HUB implementation and will not have any negative effects on network operation.

When no activity appears on the HUB ports, the HUB enters the idle state and all receivers are enabled. This state corresponds to a clear condition within the octal register which provides disable signals to the transmitters of all ports through the interface modules. As soon as any port senses activity (port n), one of 8 74S74's is clocked low causing the output of AND 1 to go low. This in turn brings the signal SET to a high which causes the octal register to be clocked through AND 2. The clocking of the octal register causes one output to remain low (the one corresponding to the port which sensed activity designated as port n) and the other seven outputs to go high. This allows port n to transmit (repeat) its signal to all other ports. For each pulse sensed, the delay module will generate $\overline{\text{PULSE 1}}$ and $\overline{\text{PULSE 2}}$ which is used by all other ports to generate the dipulse as shown in figure 7. The HUB remains in this active state until the transmission it is repeating is finished. At this time it returns to the idle state.

The determination of when a transmission is finished is based on time. There are never more than nine consecutive spacing elements in a transmission (the start element and eight zeros). Therefore, a dipulse is received at least once every ten unit intervals (4 microseconds). The COM 9026 has a turnaround time somewhat greater than 12 microseconds so there will be at least a 12 microsecond interval of no activity between the end of the last data element of one transmission and the start of the alert burst of the next transmission. Were it not for the potential reflection problem caused by an unterminated or unconnected length of coax, the HUB could drop back into the idle state when the receiver has not heard anything for some period of time between 4 and 12 microseconds.

In order to provide protection against reflections, the HUB should not fall back into the idle state until any and all reflections cease. For individual runs of coax not greater than 2000 feet (RG62 coax), a reflection from a shorted or unterminated cable will return in less than 4.9 microseconds. Changing the 4 microsecond limit to 4.9 microseconds will allow the HUB and the network to be unaffected by reflections. For the duration of the packet, retriggerable one shot OS1 will never fire. The 5.5 microsecond duration of OS1 will determine when a packet transmission has concluded by sensing a lack of activity for greater than 4.9 microseconds. When OS1 fires, OS2 produces a 150 nanosecond pulse which resets the octal register, resets the signal SET and clears all 8 74S74's. This corresponds to the idle state of the HUB and the process repeats when the next packet is received.

It is possible to implement a passive HUB as shown in figure 12. This arrangement allows for a maximum of 4 ports. For proper operation, each port must be terminated in 93 ohms either by connecting it to an active node or attaching a 93 ohm BNC terminator to the unconnected port. When the ports are terminated properly, each port will have an input impedance of 93 ohms. Due to the considerable loss experienced in this arrangement, it is recommended that no more than 4 nodes be connected in this manner.

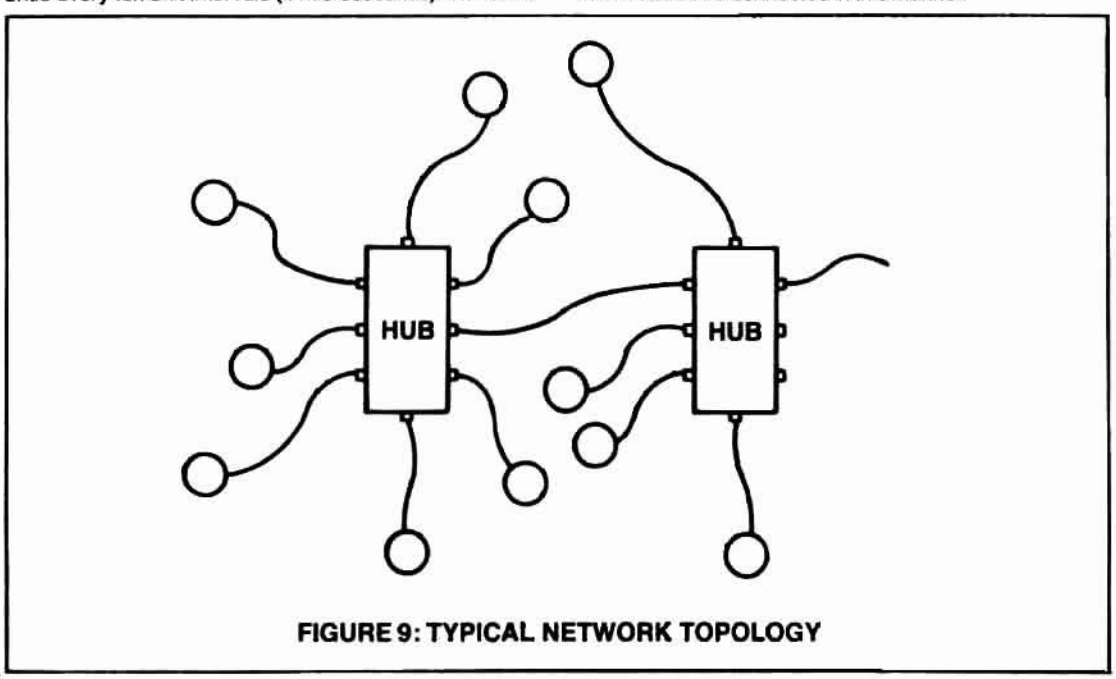


FIGURE 9: TYPICAL NETWORK TOPOLOGY

Data Sheets

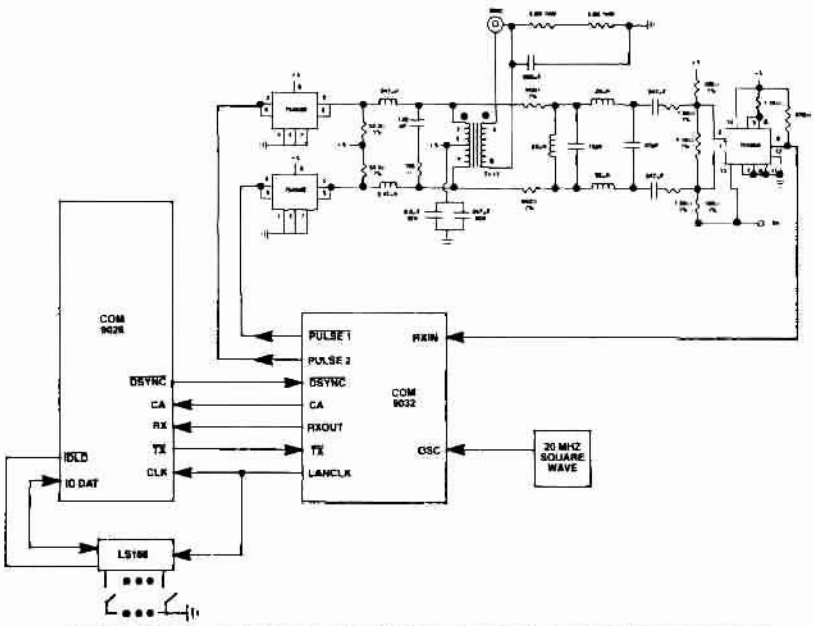
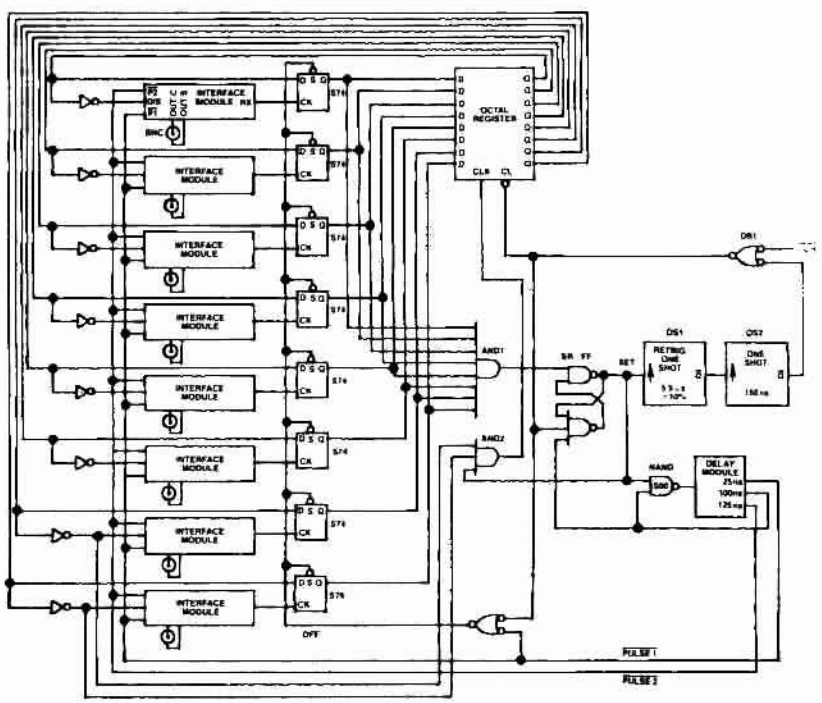
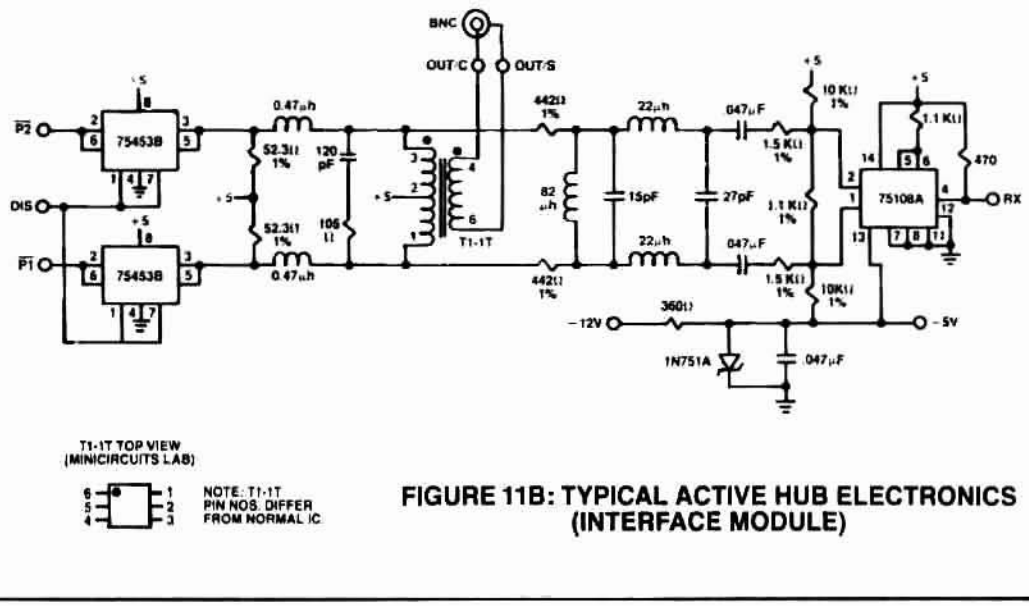


FIGURE 10: ARCNET* COMPATIBLE CABLE TRANSCEIVER USING THE COM 9032



*ARCNET is a registered trademark of the Datapoint Corporation



T1-1T TOP VIEW
(MINICIRCUITS LAB)

NOTE: T1-1T PIN NOS. DIFFER FROM NORMAL IC

FIGURE 11B: TYPICAL ACTIVE HUB ELECTRONICS (INTERFACE MODULE)

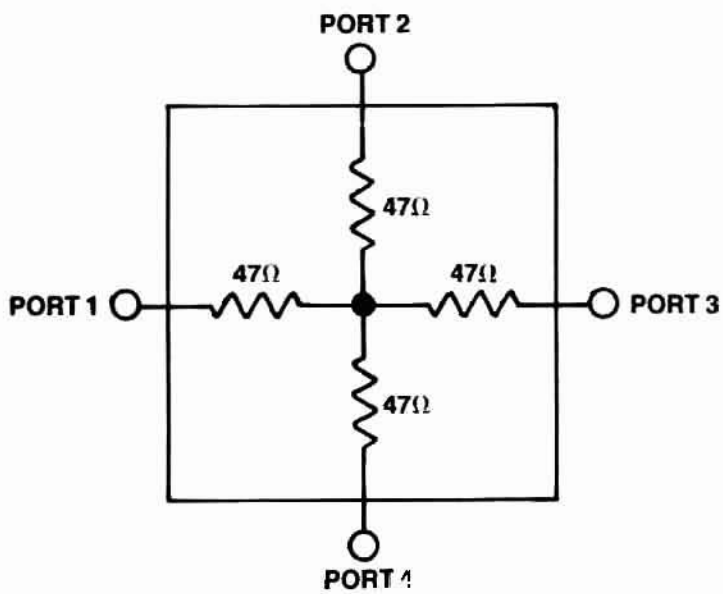


FIGURE 12: 4 PORT PASSIVE HUB

PROGRAMMING THE COM 9026

Packet Transmission

Transmission of a message begins with the processor selecting a page in the RAM buffer and writing the packet. Figure 13 illustrates the RAM buffer format for a message of length 120 (78 HEX) from ID #4C HEX to ID #B2 HEX. Note that address 02 of the selected page contains the 2's complement of the number of data bytes in the message. Figure 14 illustrates the RAM buffer format for a message of length 300 (12C HEX; long packet) from ID #2F to ID #D8. Note that address 02 must contain all zeros with address 03 equal to the 2's complement of the number of data bytes in the message. The 2's complement for long packets is calculated with respect to 512 but only 8 bits are used in RAM buffer address 03. The COM 9026 will keep track of the 9th bit internally. The RAM buffer is arranged such that the last data byte will always reside in address 255 (FF HEX) for short packets and address 511 (1FF HEX) for long packets. Broadcast messages will be transmitted if address 01 is set to 00.

Once the buffer is loaded, the processor must wait for the TA status bit to become a logic one. The TA bit informs the processor that a previous transmit command has concluded and another transmit command can be issued. Each time the message is loaded and a transmit command issued, it will take a variable amount of time before the message is transmitted depending on the traffic on the network and the location of the token at the time the transmit command was issued. Typically, the conclusion of the transmit command, which is flagged when TA becomes a logic one, generates an interrupt. While waiting for the interrupt to occur, the processor can load another page in the RAM buffer with the next message to be sent in anticipation of the transmitter becoming available (TA becomes a logic one). In this way, double buffering is accomplished by loading a second message while the first message is being transmitted. The interrupt will then allow the software to time the repeated issuing of transmit commands.

Before a message is transmitted, the destination node is asked if it is able to receive the message via a FREE BUFFER ENQUIRY transmission. This is done automatically by the COM 9026 with no software intervention. If the destination node is not servicing its COM 9026, for whatever reason, the receiver at the destination node will be inhibited (RI set to a logic one) and the source node will never be able to deliver the packet and set the TA bit to a logic one. Because of this, there should be a software timeout on the TA bit. When the timer times out, the processor should disable the transmitter which forces the COM 9026 to abandon the transmission and causes the TA bit to set to a logic one when the node next receives the token. If the source node attempts to transmit a packet to a nonexistent node, the packet will never be delivered but the TA bit will always be set to a logic one. In this situation, the TMA bit will never get set.

If the disable transmitter command does not cause the TA bit to be set in the time it takes the token to make a round trip through the network, it will indicate one of three situations;

1-The node is disconnected from the network.
2-There are no other active nodes on the network.
3-The external receive circuitry has failed.

These situations can be determined by using another software timeout which is greater than the worst case time for a round trip token pass which occurs when all nodes transmit a maximum length message.

It should be noted that each node, upon packet transmission, ignores the value of the SID in the buffer and instead inserts the ID number as specified by the external switches.

Packet Reception

To enable the receiver for packet reception, the processor selects a page in the buffer to use and waits for the RI status bit to become a logic one. The RI bit informs the processor that a previous RECEIVE command has concluded and another RECEIVE command can be issued. Each time a receive command is issued, the reception can take a variable length of time since there is no way of telling when another node will decide to transmit a message directed at this node. The RECEIVE command will reserve a particular page of memory in the RAM buffer for reception. Only the successful reception of a packet, or the issuing of a DISABLE RECEIVE command will set the RI bit to a logic one, thus freeing up the page in the RAM buffer for processor accesses.

ADDRESS	DATA
00	4C
01	B2
02	88(= 100-78)
:	:
:	:
:	:
88	DATA BYTE 1
89	DATA BYTE 2
8A	DATA BYTE 3
:	:
:	:
:	:
FF	DATA BYTE 120

FIGURE 13: TYPICAL SHORT PACKET BUFFER FOR TRANSMIT

ADDRESS	DATA
00	2F
01	D8
02	00
03	D4(= 200-12C)
:	:
:	:
D4	DATA BYTE 1
D5	DATA BYTE 2
D6	DATA BYTE 3
:	:
:	:
:	:
1FF	DATA BYTE 300

FIGURE 14: TYPICAL LONG PACKET BUFFER FOR TRANSMIT

Typically, the conclusion of a RECEIVE command, which is flagged by the RI bit being set to a logic one, will generate an interrupt and allow the processor to read or operate on the message as required. Figure 15 illustrates the contents of a page in the RAM buffer after a packet is received for a source ID # of F3 and a destination ID # of 91 with a packet length of 201 bytes (C9 HEX). Figure 16 illustrates the contents on the RAM buffer after a packet is received from a source ID # of C3 and a destination ID # of 1F with a packet length of 490 bytes (1EA HEX). The COM 9026 will deposit packets in the RAM buffer in a format identical to the transmit format allowing for a message to be received and then retransmitted without rearranging any bytes in the RAM buffer.

COM 9026 Interrupts

When using the interrupt structure of the COM 9026 to time the issuing of the transmit and receive commands, certain procedures should be followed. The INT output of the COM 9026 is generated in a variety of ways. For the transmitter, the INT output is generated by the logic function TA anded with bit zero in the interrupt mask register. Assuming the mask register bit is set to a logic one, allowing transmitter interrupts to occur, when the TA bit gets set to a logic one, the interrupt is simultaneously generated. In order to clear the interrupt and prevent repeated servicing of the same interrupt, either another transmit command should be loaded (if there is another message ready to be transmitted) which will reset the TA bit to a logic zero, or bit zero of the interrupt mask register should be reset to a logic zero.

During reception, the INT output is generated by the logic function RI anded with bit 7 of the interrupt mask register. Assuming the mask register bit 7 is set to a logic one, allowing receive interrupts to occur, when the RI bit gets set to a logic one, an interrupt is simultaneously generated. As for the transmitter, the interrupt should be cleared during the interrupt service routine. The clearing of the interrupt is accomplished by either issuing another receive command (if a page in the RAM buffer has been freed up to accept a new data packet) or by resetting bit 7 of the interrupt mask register to a logic zero.

Network Performance

The most important parameter used to measure performance in a local area network is the amount of time a node has to wait before being able to send a message. This parameter actually denotes the number of messages per second leaving each node. In the token passing scheme used by the COM 9026, this wait time is bounded by the time it takes the token to make a round trip through each node on the network. This time is a function of the number of nodes on the network, the traffic activity, and the number of bytes transmitted in each message. There are also some delay times that are intrinsic to the COM 9026 contributing to this wait time.

The COM 9026 will perform a simple token pass (it receives the token, has nothing to transmit and passes the token to the Next ID) in approximately 28 microseconds. Therefore, the best time for a round trip token pass to each node can be expressed as follows:

$$Tb = 28N \text{ microseconds}$$

where N equals the number of nodes on the network. When a particular node receives the token and has a message to transmit, the COM 9026 introduces an additional time of 113 microseconds plus 4.4 microseconds for each byte transmitted in the message. Therefore, the worst case time for a round trip token pass, which exists when each node on the network has a message to transmit, can be expressed as follows:

$$Tw = Tb + (113 + 4.4B)N \text{ microseconds}$$

where B equals the average number of bytes sent per message. Combining terms, the wait time, Twait, is bounded by the following equation:

$$28N < Twait < (141 + 4.4B)N \text{ microseconds}$$

In a typical network consisting of 10 nodes with an average message length of 100 bytes, Twait will fall between 280 microseconds (no messages sent) and 5.81 milliseconds (when all 10 nodes send 100 byte messages). If only a single node is sending messages, it can send one every 833 microseconds; a rate of 1200 messages per second or 120,000 bytes per second. If all 10 nodes send 100 byte messages, each node will be able to send a message every 5.81 milliseconds; a rate of 172 messages per second or 17,200 bytes per second.

In actual practice, Datapoint Corporation has installed many ARCNET systems with as many as 200 nodes active at any given time. A typical network supports two totally independent operating systems and a wide variety of uses including program loading, word processing, print spooling, program development, electronic mail, etc. The traffic load on this type network rarely falls below 400 messages

ADDRESS	DATA
00	F3
01	91
02	37(= 100-C9)
:	:
37	DATA BYTE 1
38	DATA BYTE 2
39	DATA BYTE 3
:	:
FF	DATA BYTE 201

FIGURE 15: TYPICAL SHORT PACKET BUFFER AFTER RECEPTION

ADDRESS	DATA
00	C3
01	1F
02	00
03	16(=200-1EA)
:	:
16	DATA BYTE 1
17	DATA BYTE 2
18	DATA BYTE 3
:	:
1FF	DATA BYTE 490

FIGURE 16: TYPICAL LONG PACKET BUFFER AFTER RECEPTION

per second, yet less than 2% of the nodes send a message on any single token trip. The time required for a token trip, therefore, stays very close to the no traffic value with peaks of three times the no traffic value being extremely rare.

The COM 9026 has some interesting features that allow one to monitor the dynamic performance of the network from any node. During any message transmission, each node will receive the source ID (SID) and destination ID (DID) and store the SID into RAM buffer location 02 of the current page enabled for receive. If the message is not directed at the particular node, the message itself is not deposited into the RAM buffer. Every node, therefore, will store at least the source of every message sent on the network making it possible to monitor the traffic activity.

In addition, continual loading of a TRANSMIT command followed immediately by a DISABLE TRANSMIT command makes it possible to measure the time for one complete token pass. Once the DISABLE TRANSMIT command is loaded, the command will not actually end until the node next receives the token. In this case, the TA bit in the status register is used to inform the host processor that the token has been passed through the node since only receipt of the token will allow the DISABLE TRANSMIT command to be completed. By measuring the time between successive settings of the TA status bit, an accurate measure of the time for every round trip token pass can be determined.

A NETWORK RECONFIGURATION occurs whenever a new network node is first activated onto the system. In the normal course of events, nodes are always being activated, and the system adjusts this by initiating a NETWORK RECONFIGURATION. The time to complete a NETWORK RECONFIGURATION and return to a normal operating environment is a function of the propagation delay between nodes, the number of nodes on the network, and the highest ID number on the network. Figure 17 is a graph illustrating the reconfiguration time as a function of the number of nodes on the network and the highest ID number and shows a range of 21 to 61 milliseconds. The reconfiguration time shown assumes no cable propagation delay. The reconfiguration time has no long lasting effect on the system performance and will only increase the time of a single token pass by the actual time of reconfiguration.

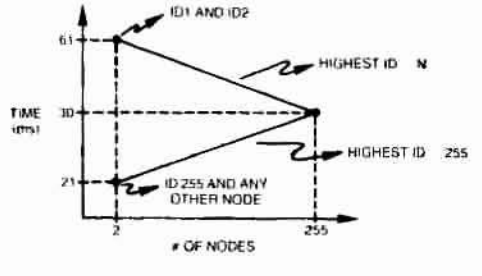


FIGURE 17:
NETWORK RECONFIGURATION TIME

Similarly, when a node is deactivated, the node that usually passes the token will have to continually try to pass the token to the next highest ID. The time it takes for a node to pass the token and find the next active node is a function of the difference in ID numbers of the deactivated node and the next highest active node. For example, if node #3 passes to node #10 and node #10 passes to node #20, and if node #10 is deactivated, then node #3 will issue an INVITATION TO TRANSMIT to nodes 10, 11, 12,...etc. and finally node 20 where it will detect line activity and complete the token pass. In this example, node #3 will issue eleven INVITATION's TO TRANSMIT, all but the last one taking 93.6 microseconds (see appendix 1; TOKEN PASS with no response), before finally finding activity at node #20. In this example, the extra time associated with this system adjustment will be 10 times 93.6 microseconds plus the response time of the active node which must be less than 74 microseconds assuming a one way cable propagation delay of 31 microseconds. Just as with the NETWORK RECONFIGURATION, this adjustment has no long lasting effect on the system performance and will only increase the time of a single token pass by an amount equal to the time taken to find the next active node on the network.

For a more detailed discussion of the critical performance parameters, refer to appendix 1.

Extended Length Message Operation

The COM 9026 can transmit and receive short packets (maximum length of 253 bytes) or long packets (maximum length of 508 bytes). When only short packets are used, it is possible to use either a 1K or 2K RAM buffer. When both long and short packets are used, a 2K RAM buffer must be used.

Use of the extended length message feature is controlled via the DEFINE CONFIGURATION command. This command allows the user to set the long packet enable flag. When this flag is set and the contents of RAM buffer address 02 is zero, the packet is treated as a long packet with RAM buffer address 03 pointing to the address containing the first byte in the message. In this case, the last byte in the message resides in RAM buffer address 511. When the long packet enable flag is set, both long and short packets can be handled. However, when the long packet enable flag is reset, only short packets can be handled.

Whatever the packet length, the COUNT byte will always point to an address situated in the first 256 bytes of the page selected. Because of this, message lengths of 254 through 256 bytes must be padded out to a length of at least 257 bytes in order to be handled.

Nodes equipped and configured for extended length messages can coexist in the same system as nodes not configured for extended length messages. The DEFINE CONFIGURATION command merely informs the COM 9026 of the existence of an external 2K buffer and thus need only be issued at initialization time. Operation with standard length messages (less than 254 bytes) proceeds in the normal fashion.

If an extended length message is sent to a node that does not have its long packet enable flag set, the receiver will ignore it. The transmitting COM 9026 will set its TA bit but not the TMA bit. If an attempt is made to have a node transmit an extended length message when the node does not have its long packet enable flag set, the packet will not be sent and the TA bit will stay off until a DISABLE TRANSMITTER command is issued. To the host processor, this situation will appear exactly as if a transmission were attempted to a node that has its receiver inhibited.

APPENDIX 1: DETAILED TIMING INFORMATION

The following information is provided for the benefit of users wishing to perform their own performance analysis. The equations shown in the section entitled NETWORK PERFORMANCE have assumed no cable propagation delay. The information that follows will accurately include all cable delays.

The lengths of the five types of COM 9026 transmissions are shown below:

INVITATIONS TO TRANSMIT (ITT)

ALERT BURST	=	2.4 µs (6 bits)
EOT, DID, DID	=	13.2 µs (33 bits)
		15.6 µs

FREE BUFFER ENQUIRIES (FBE)

ALERT BURST	=	2.4 µs (6 bits)
ENQ, DID, DID	=	13.2 µs (33 bits)
		15.6 µs

PACKETS (PAC)

ALERT BURST	=	2.4 µs (6 bits)
SOH, SID, DID, DID, COUNT	=	22.0 µs (55 bits)
B CHARACTERS	=	4.4B µs (55B bits)
CRC, CRC	=	8.8 µs (22 bits)
		33.2 µs + 4.4B µs

ACKNOWLEDGEMENTS (ACK)

ALERT BURST	=	2.4 µs (6 bits)
ACK	=	4.4 µs (11 bits)
		6.8 µs

NEGATIVE ACKNOWLEDGEMENTS (NAK)

ALERT BURST	=	2.4 µs (6 bits)
NAK	=	4.4 µs (11 bits)
		6.8 µs

In addition, there are certain delay constants and cable propagation times required for analysis as described below:

CHIP TURNAROUND TIME (Tta) = 12.6 µs

This time is defined as the time from the end of any received transmission until the start of a response.

TOKEN PROPAGATION DELAY (Tpt)

This time is defined as the CABLE propagation time between the node holding the token and the node receiving the token.

MESSAGE PROPAGATION TIME (Tpm)

This time is defined as the CABLE propagation time between the node holding the token and the node receiving a message.

BROADCAST DELAY TIME (Tbd) = 15.6 µs

This time is defined as the time from the end of a transmitted broadcast packet until the start of a token pass.

RESPONSE TIMEOUT (Trp)

This time is the maximum amount of a time a COM 9026 will wait for a response which should be greater than or equal to twice the maximum cable propagation delay (the delay between the two furthest nodes) plus the CHIP TURNAROUND TIME as defined above. This value is programmable using the ET1 and ET2 inputs.

RECOVERY TIME (Trc) = 3.4 µs

This time is the amount from the end of the RESPONSE TIMEOUT until the start of a token pass.

Given the above numbers, it is possible to calculate the time a token will "dwell" at any node. A number of cases are detailed below. In each case, the time calculated is the time from the start of one token pass to the start of the next token pass. For all cases a Trp of 74.6 µs is assumed.

SIMPLE TOKEN PASS (no message sent)

ITT	15.6 µs
Tta	12.6 µs + Tpt
	28.2 µs + Tpt

TOKEN PASS AND MESSAGE

ITT	15.6 µs
Tta	12.6 µs + Tpt
FBE	15.6 µs
Tta	12.6 µs + Tpm
ACK	6.8 µs
Tta	12.6 µs + Tpm
PAC	33.2 µs + 4.4B µs
Tta	12.6 µs + Tpm
ACK	6.8 µs
Tta	12.6 µs + Tpm
	141.0 µs + 4.4B µs + Tpt + 4Tpm

TOKEN PASS AND MESSAGE (receiver inhibited)

ITT	15.6 µs
Tta	12.6 µs + Tpt
FBE	15.6 µs
Tta	12.6 µs + Tpm
NAK	6.8 µs
Tta	12.6 µs + Tpm
	75.8 µs + Tpt + 2Tpm

TOKEN PASS AND MESSAGE (broadcast)

ITT	15.6 µs
Tta	12.6 µs + Tpt
PAC	33.2 µs + 4.4B µs
Tbd	15.6 µs
	77.0 µs + 4.4B µs + Ttp

TOKEN PASS AND MESSAGE (ACK gets lost)

ITT	15.6 µs
Tta	12.6 µs + Tpt
FBE	15.6 µs
Tta	12.6 µs + Tpm
ACK	6.8 µs
Tta	12.6 µs + Tpm
PAC	33.2 µs + 4.4N µs
Trp	74.6 µs
Trc	3.4 µs
	187.0 µs + 4.4B µs + Tpt + 2Tpm

TOKEN PASS AND MESSAGE (destination node does not exist)

ITT	15.6 µs
Tta	12.6 µs + Tpt
FBE	15.6 µs
Trp	74.6 µs
Trc	3.4 µs
	121.8 µs + Tpt

TOKEN PASS (no response)

ITT	15.6 µs
Trp	74.6 µs
Trc	3.4 µs
	93.6 µs

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, NY 11788 (516) 273-3100

STANDARD MICROSYSTEMS CORPORATION

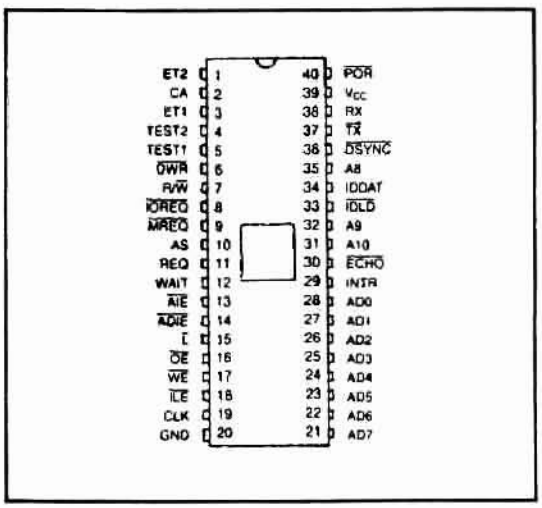
COM 9026

Local Area Network Controller LANC™

FEATURES

- ☐ 2.5 M bit data rate
- ☐ ARCNET* local area network controller
- ☐ Modified token passing protocol
- ☐ Self-reconfiguring as nodes are added or deleted from network
- ☐ Handles variable length data packets
- ☐ 16 bit CRC check and generation
- ☐ System efficiency increases with network loading
- ☐ Standard microprocessor interface
- ☐ Supports up to 255 nodes per network segment
- ☐ Ability to interrupt processor at conclusion of commands
- ☐ Interfaces to an external 1K or 2K RAM buffer
- ☐ Arbitrates buffer accesses between processor and COM 9026
- ☐ Replaces over 100 MSI/SSI parts
- ☐ Ability to transmit broadcast messages
- ☐ Compatible with broadband or baseband systems
- ☐ Compatible with any interconnect media (twisted pair, coax, etc.)

PIN CONFIGURATION



- ☐ Arbitrary network configurations can be used (star, tree, etc.)
- ☐ Single + 5 volt supply

GENERAL DESCRIPTION

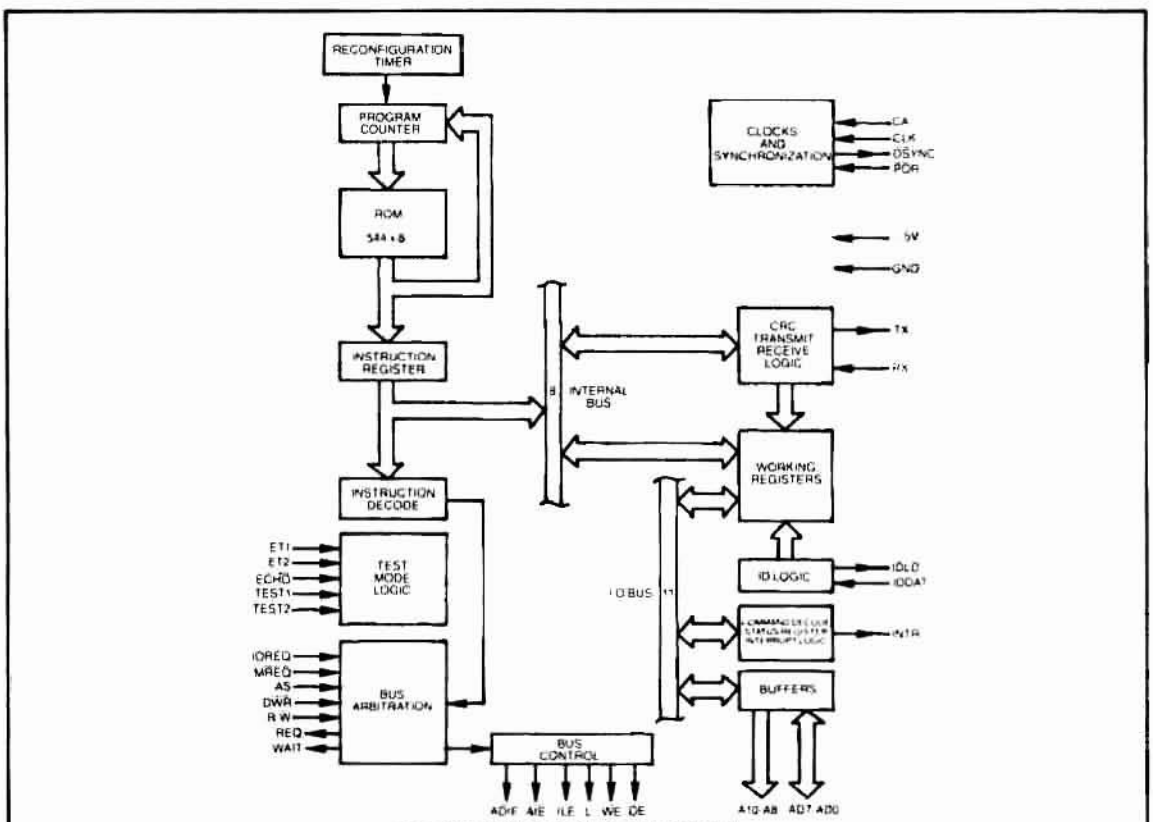
The COM 9026 is a special purpose communications adapter for interconnecting processors and intelligent peripherals using the ARCNET local area network. The ARCNET local area network is a self-polling "modified token passing" network operating at a 2.5 M bit data rate. A "modified token passing" scheme is one in which all token passes are acknowledged by the node accepting the token. The token passing network scheme avoids the fluctuating channel access times caused by data collisions in so-called CSMA/CD schemes such as Ethernet.

The COM 9026 circuit contains a microprogrammed sequencer and all the logic necessary to control the token passing mechanism on the network and send and receive data packets at the appropriate time. A maximum of 255 nodes may be connected to the network with each node being assigned a unique ID.

The COM 9026 establishes the network configuration, and automatically re-configures the network as new nodes are added or deleted from the network. The COM 9026 performs address decode, CRC checking and generation, and packet acknowledgement, as well as other network management functions. The COM 9026 interfaces directly to the host processor through a standard multiplexed address/data bus.

An external RAM buffer of up to 2K locations is used to hold up to four data packets with a maximum length of 508 bytes per message. The RAM buffer is accessed both by the processor and the COM 9026. The processor can write commands to the COM 9026 and also read COM 9026 status. The COM 9026 will provide all signals necessary to allow smooth arbitration of all RAM buffer operations.

*ARCNET is a registered trademark of the Datapoint Corporation.



COM 9026 BLOCK DIAGRAM

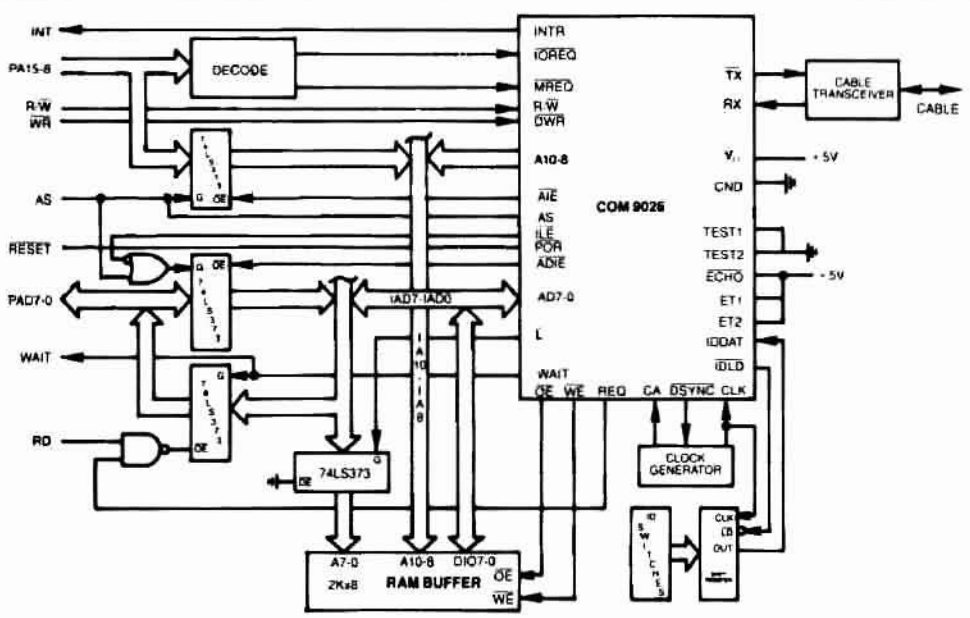


FIGURE 2—TYPICAL COM 9026 INTERFACE

Data Sheets

DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

PIN NO.	NAME	SYMBOL	FUNCTION
31, 32, 35	ADDRESS 10, 9, 8	A10, A9, A8	These three output signals are the three most significant bits of the RAM buffer address. These signals are in their high impedance state except during COM 9026 access cycles to the RAM buffer. A10 and A9 will take on the value nn as specified in the ENABLE RECEIVE or ENABLE TRANSMIT commands to or from page nn and should be viewed as page select bits. For packets less than 256 bytes a 1K buffer can be used with A8 unconnected. For packets greater than 256 bytes, a 2K buffer is needed with A8 connected.
21, 22, 23, 24, 25, 26, 27, 28	ADDRESS/ DATA 7-0	AD7-AD0	These 8 bidirectional signals are the lower 8 bits of the RAM buffer address and the 8 bit data path in and out of the COM 9026. AD0 is also used for I/O command decoding of the processor control or status commands to the COM 9026
8	I/O REQUEST	$\overline{IOREQ}$	This input signal indicates that the processor is requesting the use of the data bus to receive status information or to issue a command to the COM 9026. This signal is sampled internally on the falling edge of AS.
9	MEMORY REQUEST	$\overline{MREQ}$	This input signal indicates that the processor is requesting the use of the data bus to transfer data to or from the RAM buffer. This signal is sampled internally on the falling edge of AS.
7	READ/WRITE	R/$\overline{W}$	A high level on this input signal indicates that the processor's access cycle to the COM 9026 or the RAM buffer will be a read cycle. A low level indicates that a write cycle will be performed to either the RAM buffer or the COM 9026. The write cycle will not be completed, however, until the $\overline{DWR}$ input is asserted. This signal is an internal transparent latch gated with AS.
10	ADDRESS STROBE	AS	This input signal is used by the COM 9026 to sample the state of the $\overline{IOREQ}$, $\overline{MREQ}$ and R/$\overline{W}$ inputs. The COM 9026 bus arbitration is initiated on the falling edge of this signal.
11	REQUEST	REQ	This output signal acknowledges the fact that the processor's I/O or memory cycle has been sampled. The signal is equal to $\overline{MREQ}$ or $\overline{IOREQ}$ passed through an internal transparent latch gated with AS.
12	WAIT	$\overline{WAIT}$	This output signal is asserted by the COM 9026 at the start of a processor access cycle to indicate that it is not ready to transfer data. WAIT returns to its inactive state when the COM 9026 is ready for the processor to complete its cycle.
6	DELAYED WRITE	$\overline{DWR}$	This input signal informs the COM 9026 that valid data is present on the processor's data bus for write cycles. The COM 9026 will remain in the WAIT state until this signal is asserted. $\overline{DWR}$ has no effect on read cycles. If the processor is able to satisfy the write data setup time, it is recommended that this signal be grounded.
29	INTERRUPT REQUEST	INTR	This output signal is asserted when an enabled interrupt condition has occured. INTR returns to its inactive state by resetting the interrupting status condition or the corresponding interrupt mask bit.
18	INTERFACE LATCH ENABLE	$\overline{ILE}$	This output signal, in conjunction with $\overline{ADIE}$, gates the processor's address/data bus (PAD7-PAD0) onto the interface address/data bus (IAD7-IAD0) during the data valid portion of a Processor Write RAM or Processor Write COM 9026 operation.
14	ADDRESS/ DATA INPUT ENABLE	$\overline{ADIE}$	This output signal enables the processor's address/data bus (PAD7-PAD0) captured by AS or $\overline{ILE}$ onto the interface address/data bus (IAD7-IAD0).
13	ADDRESS INPUT ENABLE	$\overline{AIE}$	This output signal enables the processor's upper 3 address bits (PA10-PA8) onto the interface address bus (IA10-IA8).
15	LATCH	$\overline{L}$	This output signal latches the interface address/data bus (IAD7-IAD0) into a latch which feeds the lower 8 address bits of the RAM buffer during address valid time of all RAM buffer access cycles.
17	WRITE ENABLE	$\overline{WE}$	This output signal is used as a write pulse to the external RAM buffer. Data is referenced to the trailing edge of $\overline{WE}$.
16	OUTPUT ENABLE	$\overline{OE}$	This output signal enables the RAM buffer output data onto the interface address/data bus (IAD7-IAD0) during the data valid portion of all RAM buffer read operations.
33	ID LOAD	$\overline{IDLD}$	This output signal synchronously loads the value selected by the ID switches into an external shift register in preparation for shifting the ID into the COM 9026. The shift register is clocked with the same signal that feeds the COM 9026 on pin 19 (CLK). The timing associated with this signal and IDDAT (pin 34) is illustrated in figure 19.
34	ID DATA IN	IDDAT	This input signal is the serialized output from the external ID shift register. The ID is shifted in most significant bit first. A high level is defined as a logic "1".
1, 3	EXTENDED TIMEOUT FUNCTION 2, 1	ET2, ET1	The levels on these two input pins specify the timeout durations used by the COM 9026 in its network protocol. Refer to the section entitled "Extended Timeout Function" for details.
37	TRANSMIT DATA	$\overline{TX}$	This output signal contains the serial transmit data to the CABLE TRANSCEIVER.
38	RECEIVE DATA	RX	This input signal contains the serial receive data from the CABLE TRANSCEIVER.

DESCRIPTION OF PIN FUNCTIONS (Continued)

PIN NO.	NAME	SYMBOL	FUNCTION
4, 5	TEST PIN 2 TEST PIN 1	TEST2 TEST1	These input pins are grounded for normal chip operation. These pins are used in conjunction with ET2 and ET1 to enable various internal diagnostic functions when performing chip level testing.
30	ECHO DIAGNOSTIC ENABLE	$\overline{ECHO}$	When this input signal is low, the COM 9026 will re-transmit all messages of length less than 254 bytes. This input should be tied high for normal chip operation and is only utilized when performing chip level testing.
19	CLOCK	CLK	A continuous 5 MHz clock input used for timing of the COM 9026 bus cycles, bus arbitration, serial ID input, and the internal timers.
2	CA	CA	This input signal is a 5 MHz clock used to control the operation of the COM 9026 microcoded sequencer. This input is periodically halted in the high state by the $\overline{DSYNC}$ output.
36	DELAYED SYNC	$\overline{DSYNC}$	This output signal is asserted by the COM 9026 to cause the external clock generator logic to halt the CA clock. Refer to figure 9.
40	POWER ON RESET	$\overline{POR}$	This input signal clears the COM 9026 microcoded sequencer program counter to zero and initializes various internal control flags and status bits. The POR status bit is also set which causes the INTR output to be asserted. Repeated assertion of this signal will degrade the performance of the network.
39	+5 VOLT SUPPLY	V_{CC}	Power Supply
20	GROUND	GND	Ground

PROTOCOL DESCRIPTION

LINE PROTOCOL DESCRIPTION

The line protocol can be described as isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. Each byte will take up exactly 11 clock intervals with a single clock interval being 400 nanoseconds in duration. As a result, 1 byte is transmitted every 4.4 microseconds and the time to transmit a message can be exactly determined. The line idles in a spacing (logic 0) condition. A logic '0' is defined as no line activity and a logic 1 is defined as a pulse of 200 nanoseconds duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic 1). Eight bit data characters are then sent with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be sent as described below:

Invitations To Transmit

An ALERT BURST followed by three characters; an EOT (end of transmission—ASCII code 04 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to pass the token from one node to another.

Free Buffer Enquiries

An ALERT BURST followed by three characters; an ENQ (ENQuiry—ASCII code 05 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to ask another node if it is able to accept a packet of data.

Data Packets

An ALERT BURST followed by the following characters:

- — an SOH (start of header-ASCII code 01 HEX)
- —a SID (Source IDentification) character
- —two (repeated) DID (destination IDentification) characters.
- —a single COUNT character which is the 2's complement of the number of data bytes to follow if a "short packet" is being sent or 00 HEX followed by a COUNT character which is the 2's complement of the number of data bytes to follow if a "long packet" is being sent.
- —N data bytes where COUNT = 256-N (512-N for a "long packet")
- —two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is $X^{16} + X^{15} + X^2 + 1$.

Acknowledgements

An ALERT BURST followed by one character; an ACK (ACKnowledgement—ASCII code 06 HEX) character. This message is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES.

Negative Acknowledgements

An ALERT BURST followed by one character; a NAK (Negative AcKnowledgement—ASCII code 15 HEX). This message is used as a negative response to FREE BUFFER ENQUIRIES.

NETWORK PROTOCOL DESCRIPTION

Communication on the network is based on a "modified token passing" protocol. A "modified token passing" scheme is one in which all token passes are acknowledged by the node receiving the token. Establishment of the network configuration and management of the network protocol are handled entirely by the COM 9026's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the RAM buffer, and issuing a command to enable the transmitter. When the COM 9026 next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16 bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node will verify the packet.

If the packet is received successfully, the receiving node transmits an acknowledge message (or nothing if it is received unsuccessfully) allowing the transmitter to set the appropriate status bits to indicating successful or unsucessful delivery of the packet. An interrupt mask permits the COM 9026 to generate an interrupt to the processor when selected status bits become true. Figure 3 is a flow chart illustrating the internal operation of the COM 9026.

NETWORK RECONFIGURATION

A significant advantage of the COM 9026 is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated a NETWORK RECONFIGURATION is performed. When a new COM 9026 is turned on (creating a new active node on the network), or if the COM 9026 has not received an INVITATION TO TRANSMIT for 840 milliseconds, it causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line. It also provides line activity which allows the COM 9026 sending the INVITATION TO TRANSMIT to release control of the line.

When any COM 9026 sees an idle line for greater than 78.2 microseconds, which will only occur when the token is lost, each COM 9026 starts an internal time out equal to 146 microseconds times the quantity 255 minus its own ID. It also sets the internally stored NID (next ID representing the next possible ID node) equal to its own ID. If the timeout expires with no line activity, the COM 9026 starts sending INVITATIONS TO TRANSMIT with the DID equal to the currently stored NID. Within a given network, only one COM 9026 will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM 9026 waits for activity on the line. If there is no activity for 74.7 microseconds, the COM 9026 increments the NID value and transmits another INVITATION TO TRANSMIT using the new NID equal to the DID. If activity appears before the 74.7 microsecond timeout expires, the COM 9026 releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT will be sent to all 256 possible ID's. Each COM 9026 on the network will finally have saved a NID value equal to the ID of the COM 9026 that assumed control from it. From then until the next NETWORK RECONFIGURATION, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT sent to ID's not on the network. When a node is powered off, the previous node will attempt to pass it the token by issuing an INVITATION TO TRANSMIT. Since this node will not respond, the previous node will time out and transmit another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The time required to do a NETWORK RECONFIGURATION depends on the number of nodes in the network, the propogation delay between nodes and the highest ID number on network but will be in the range of 24 to 61 milliseconds.

BROADCAST MESSAGES

Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the destination ID (DID) equal to zero. Figure 8 illustrates the position of each byte in the packet with the DID residing at address 01 HEX of the current page selected in the TRANSMIT command. Each individual node has the ability to ignore broadcast messages by setting the most signficant bit of the ENABLE RECEIVE TO PAGE nn command (see "WRITE COM 9026 COMMANDS") to a logic zero.

COM 9026 OPERATION

BUFFER CONFIGURATION

During a transmit sequence, the COM 9026 fetches data from the Transmit Buffer, a 256 (or 512) byte segment of the RAM buffer. The appropriate buffer size is specified in the DEFINE CONFIGURATION command. When long packets are enabled, the COM 9026 will interpret the packet as a long or short packet depending on whether the contents of buffer location 02 is zero or non zero. During a receive sequence, the COM 9026 stores data in the receive buffer, also a 256 (or 512) byte segment of the RAM buffer. The processor I/O command which enables either the COM 9026 receiver or the COM 9026 transmitter also initializes the respective buffer page register. The formats of the buffers (both 256 and 512 byte) are shown below.

FIGURE 8— RAM BUFFER PACKET CONFIGURATION

ADDRESS	FORMAT
0	SID
1	DID
2	COUNT 256 N
	NOT USED
COUNT	DATA BYTE 1
	DATA BYTE 2
	•
	•
	•
	DATA BYTE N-1
255	DATA BYTE N
	NOT
511	USED

SHORT PACKET (256 OR 512 BYTE PAGE)

ADDRESS	FORMAT
0	SID
1	DID
2	0
3	COUNT 512 N
	NOT USED
COUNT	DATA BYTE 1
	DATA BYTE 2
	•
	•
	•
	DATA BYTE N-1
511	DATA BYTE N

LONG PACKET (512 BYTE PAGE)

N DATA PACKET LENGTH
SID SOURCE ID
DID DESTINATION ID
(0 FOR BROADCASTS)

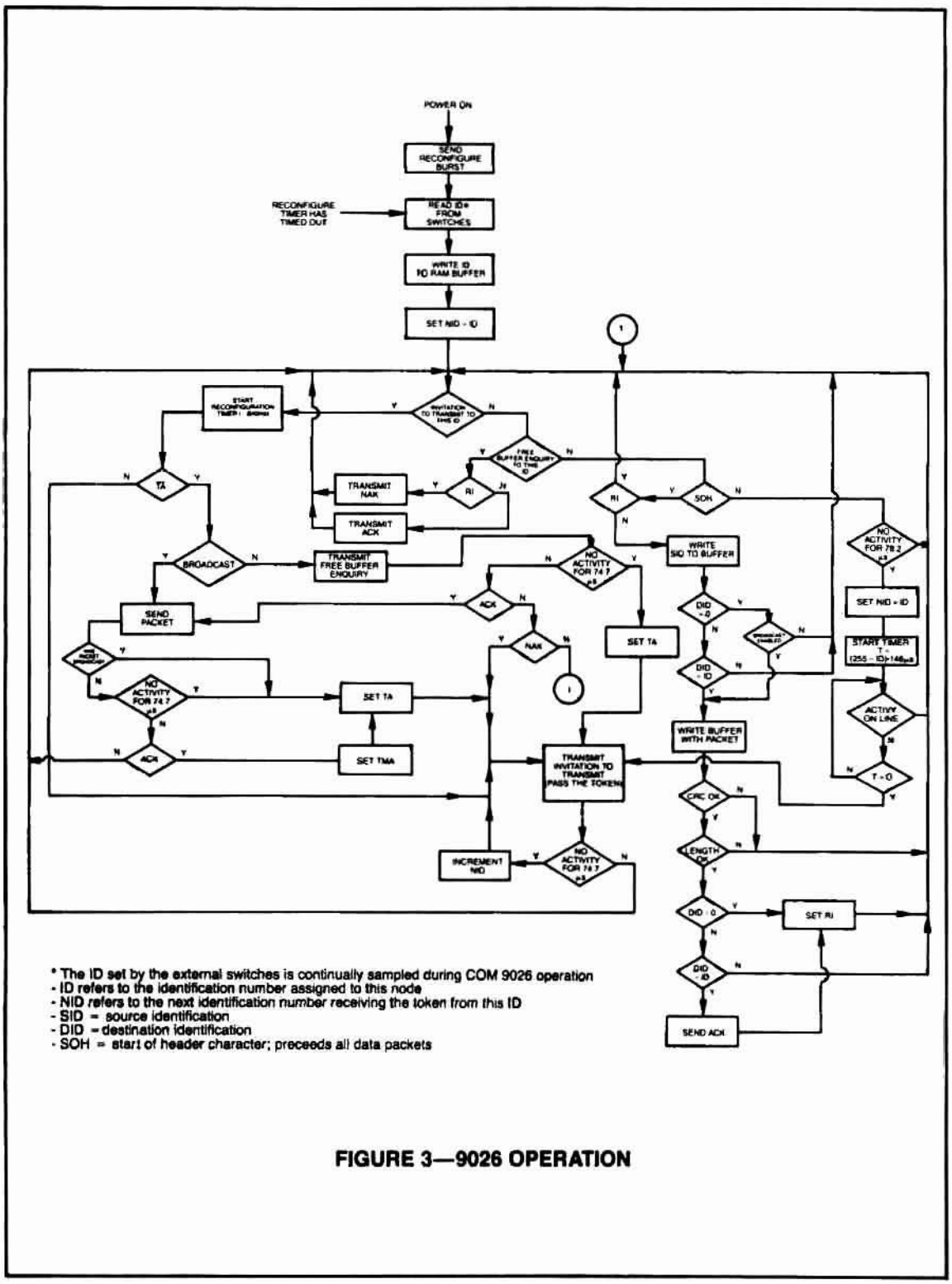


FIGURE 3—9026 OPERATION

PROCESSOR INTERFACE

Figure 2 illustrates a typical COM 9026 to processor interface. The signals on the left side of this figure represent typical processor signals with a 16 bit address bus and an 8 bit data bus with the data bus multiplexed onto the lower 8 address lines (PAD7-PAD0). The processor sees a network node (a node consists of a COM 9026, RAM buffer, cable transceiver, etc. as shown in figure 2) as 2K memory locations and 4 I/O locations within the COM 9026.

The RAM buffer is used to hold data packets temporarily prior to transmission on the network and as temporary storage of all received data packets directed to the particular node. The size of the buffer can be as large as 2K byte locations providing four pages at a maximum of 512 bytes per page. For packet lengths smaller than 256 bytes, a 1K RAM buffer can be used to provide four pages of storage. In this case address line IA8 (sourced from either the COM 9026 or the processor) should be left unconnected. Since four pages of RAM buffer are provided, both transmit and receive operations can be double buffered with respect to the processor. For instance, after one data packet has been loaded into a particular page within the RAM buffer and a transmit command for that page has been issued, the processor can start loading another page with the next message in a multimessage transmission sequence. Similarly, after one message is received and completely loaded into one page of the RAM buffer by the COM 9026, another receive command can be issued to allow reception of the next packet while the first packet is read by the processor. In general, the four pages in the RAM buffer can be used for transmit or receive in any combination. In addition, the processor will also use the interface bus (IA10-IA8, IAD7-IAD0) when performing I/O access cycles (status reads from the COM 9026 or command writes to the COM 9026).

To accomplish this double buffering scheme, the RAM buffer must behave as a dual port memory. To allow this RAM to be a standard component, arbitration and control on the interface bus (IA10-IA8, IAD7-IAD0) is required to permit both the COM 9026 and the processor access to the RAM buffer and, at the same time, permit all processor I/O operations to or from the COM 9026.

Processor access cycle requests begin on the trailing edge of AS if either $\overline{IOREQ}$ or $\overline{MREQ}$ is asserted. These access cycles run completely asynchronous with respect to the COM 9026. Because of this, upon processor access cycle requests, the COM 9026 immediately puts the processor into a wait state by asserting the WAIT output. This gives the COM 9026 the ability to synchronize and control the processor access cycle. When the processor access cycle is synchronized by the COM 9026, the WAIT signal is eventually removed allowing the processor to complete its cycle.

For processor RAM buffer access cycles, $\overline{AIE}$ and $\overline{ADIE}$ enable the processor address captured during AS time onto the interface address bus (IA10-IA8, IAD7-IAD0). The signal $\overline{L}$ will capture the 8 least significant bits of this address (appearing on IAD7-IAD0) before the data is multiplexed onto it. At the falling edge of L, a stable address is presented to the RAM buffer. For read cycles, $\overline{OE}$ allows the addressed RAM buffer data to source the interface address/data bus (IAD7-IAD0). In figure 2, this information is passed into a transparent latch gated with WAIT. At the falling edge of WAIT, the data accessed by the processor is captured

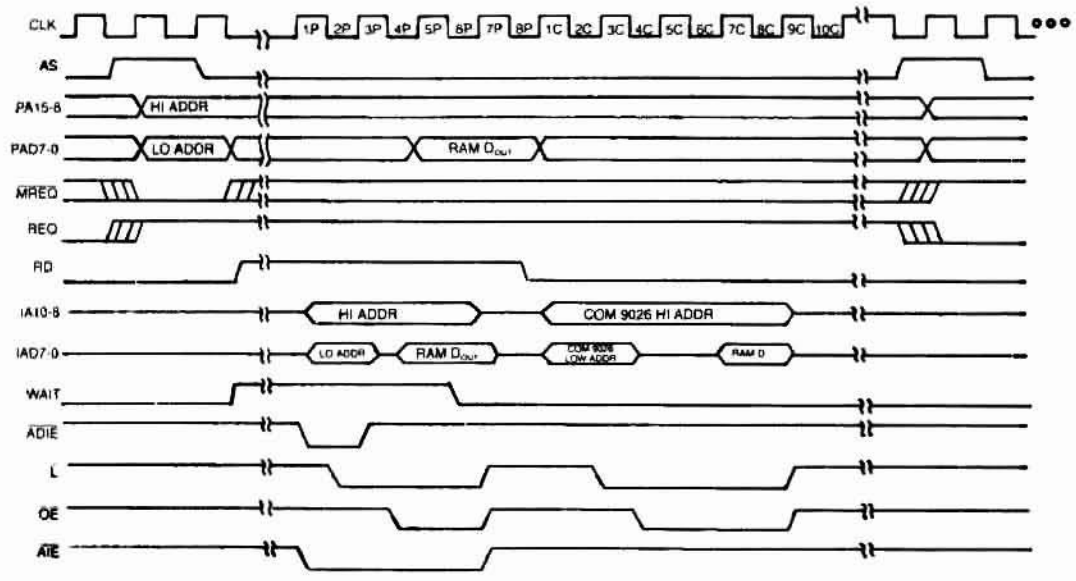


FIGURE 4—PROCESSOR READ RAM FOLLOWED BY COM 9026 READ RAM

and driven out via the logic function RD anded with REQ. For processor I/O read cycles from the COM 9026, ADIE and AIE are used to enable the processor address into the COM 9026. Data out of the COM 9026 is gated through the transparent latch and appears on the processor's data bus with the same control signals used for RAM read cycles.

For processor write cycles, after the falling edge of L, the COM 9026 produces a WE (write enable) output to the RAM buffer, and the ILE output from the COM 9026 allows the processor data to source the interface address/data bus (IAD7-IAD0). At this time the COM 9026 waits for DWR before concluding the cycle by removing the WAIT output. DWR should only be used if the processor cannot deliver the data to be written in enough time to satisfy the write setup time requirements of the RAM buffer. By delaying the activation of DWR, the period of the write cycle will be extended until the write data is valid. Since the architecture and operation of the COM 9026 requires periodic reading and writing of the RAM buffer in a timely manner, holding the DWR input off for a long period of time, or likewise by running the processor at a slow speed, can result in a data overflow condition. It is therefore recommended that if the processor write data setup time to the RAM buffer is met, then the DWR input should be grounded.

For processor I/O write cycles to the COM 9026, ADIE and AIE are used to enable the processor's address onto the interface data bus. ILE is used to enable the processor's write data into the COM 9026. Delaying the activation of DWR will hold up the COM 9026 cycle requiring the same precautions as stated for Processor RAM Write cycles.

As stated previously, processor requests occur at the falling edge of AS if either IOREQ or MREQ are active. COM 9026 requests occur when the transmitter or receiver need to read or write the RAM buffer in the course of executing the command. If the COM 9026 requests a bus cycle at the same time as the processor, or shortly after the processor, the COM 9026 cycle will follow immediately after the processor cycle. Figure 4 illustrates the timing relationship of a Processor RAM Read cycle followed by a COM 9026 RAM read cycle. Once the AS signal captures the processor address to the RAM buffer and requests a bus cycle, it takes 4 CLK periods for the processor cycle to end. Figure 4 breaks up these 4 CLK periods into 8 half clock interval labeled 1P through 8P. A COM 9026 access cycle will take 5 CLK periods to end. Figure 4 breaks up these 5 CLK periods into 10 half intervals labeled 1C through 10C.

If a processor cycle request occurs after a COM 9026 request has already been granted, the COM 9026 cycle will occur first, as shown in figure 5. Figure 5 illustrates the timing relationship of a COM 9026 RAM Write cycle followed by a Processor RAM Write cycle. Due to the asynchronous nature of the bus requests (AS and CLK), the transition from the end of the COM 9026 cycle to the beginning of the processor cycle might have some dead time. Refering to figure 5, if AS falling edge occurs after the start of half CLK interval 9C, no real contention exists and it will take between 200 and 500 nanoseconds before the processor cycle can start. The start of the processor cycle is defined as the time when the COM 9026 produces a leading edge on both ADIE and AIE. If the processor request occurs before the end of half

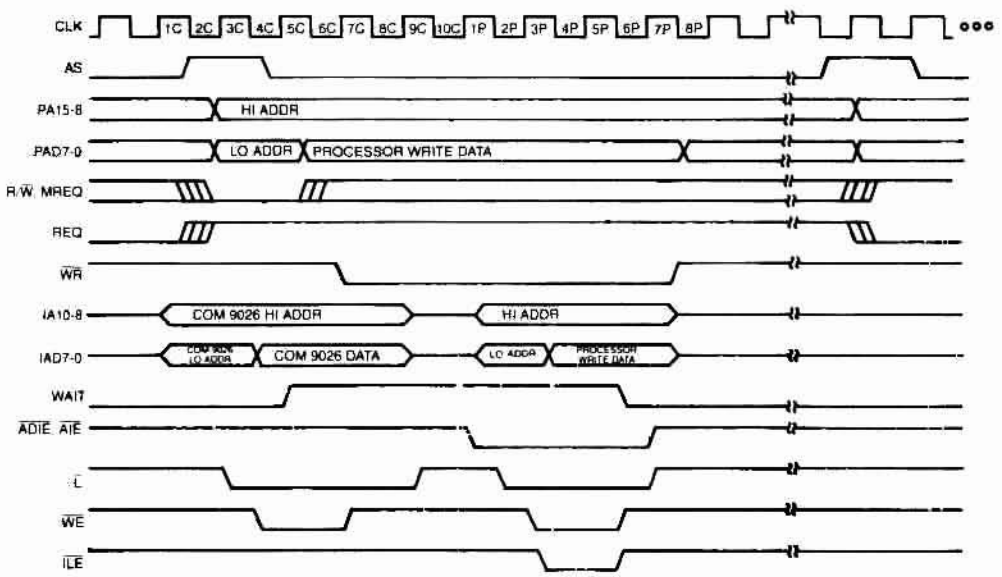


FIGURE 5—COM 9026 WRITE RAM FOLLOWED BY PROCESSOR WRITE RAM

CLK interval 5C (figure 5 illustrates this situation), then the processor cycle will always start at half CLK interval 1P. The uncertainty is introduced when the processor request occurs during half CLK intervals 6C, 7C or 8C. In this case, the processor cycle will start between 200 and 500 nanoseconds later depending on the particular timing relation between AS and CLK. The maximum time between processor request and processor cycle start, which occurs when the processor request comes just after a COM 9026 request, is 1300 nanoseconds. It should be noted that all times specified above assume a nominal CLK period of 200 nanoseconds.

Figures 6 and 7 illustrate timing for Processor Read COM 9026 and Processor Write COM 9026 respectively. These cycles are also shown divided into 8 half clock intervals (1P through 8P) and can be inserted within figures 4 and 5 if these processor cycles occur.

POWER UP AND INITIALIZATION

The COM has the following power up requirements:

1—The $\overline{\text{POR}}$ input must be active for at least 100 milliseconds.
2—The CLK input must run for at least 10 clock cycles before the POR input is removed.
3—While $\overline{\text{POR}}$ is asserted, the CA input may be running or held high. If the CA input is running, $\overline{\text{POR}}$ may be released asynchronously with respect to CA. If the CA input is held high, $\overline{\text{POR}}$ may be released before CA begins running.

During $\overline{\text{POR}}$ the status register will assume the following state:

BIT 7 (RI) set to a logic "1".
BIT 6 (ETS2) not affected
BIT 5 (ETS1) not affected
BIT 4 (POR) set to a logic "1".
BIT 3 (TEST) set to a logic "0".
BIT 2 (RECON) set to a logic "0".
BIT 1 (TMA) set to a logic "0".
BIT 0 (TA) set to a logic "1".

In addition the $\overline{\text{DSYNC}}$ output is reset inactive high and the interrupt mask register is reset (no maskable interrupts enabled). Page 00 is selected for both the receive and the transmit RAM buffer. After the $\overline{\text{POR}}$ signal is removed, the COM 9026 will generate an interrupt from the nonmaskable Power On Reset interrupt. The COM 9026 will start operation four CA clock cycles after the $\overline{\text{POR}}$ signal is removed. At this time, the COM 9026, after reading its ID from the external shift register, will execute two write cycles to the RAM buffer. Address 00 HEX will be written with the data D1 HEX and address 01 HEX will be written with the ID number as previously read from the external shift register. The processor may then read RAM buffer address 01 to determine the COM 9026 ID. It should be noted that the data pattern D1 written into the RAM has been chosen arbitrarily. Only if the D1 pattern appears in the RAM buffer can proper operation be assured.

CLOCK GENERATOR

The COM 9026 uses two separate clock inputs namely CA and CLK. The CLK input is a 5 MHz free running clock and the CA input is a start/stop clock periodically stopped and started to allow the COM 9026 to synchronize to the incoming data that appears on the RX input.

Figure 9 illustrates the timing of the CA clock generator and its relationship to the $\overline{\text{DSYNC}}$ output and the RX input. The $\overline{\text{DSYNC}}$ output is used to control the stopping of the CA clock. On the next rising edge of the CA input after $\overline{\text{DSYNC}}$ is asserted, CA will remain in the high state. The CA clock remains halted in the high state as long as the RX signal remains high. When the RX signal goes low, the CA clock is restarted and remains running until the next falling edge of $\overline{\text{DSYNC}}$. (See figure 20 for an implementation of this circuit.)

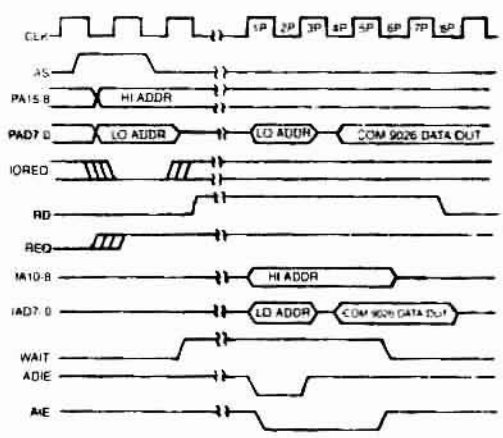


FIGURE 6—PROCESSOR READ COM 9026

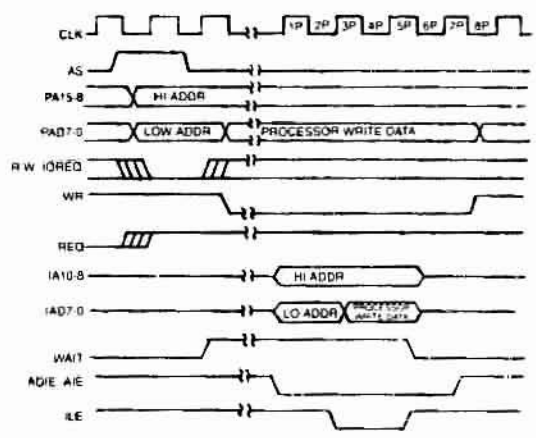


FIGURE 7—PROCESSOR WRITE COM 9026

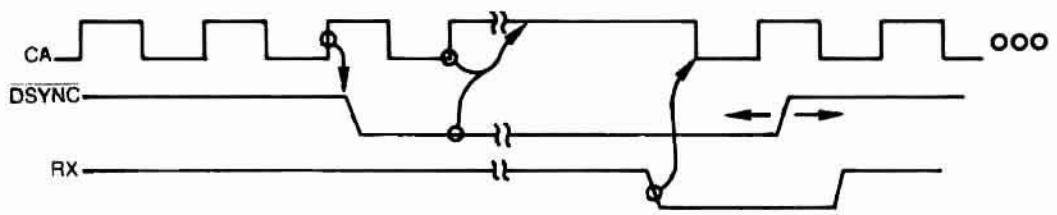


FIGURE 9—CA CLOCK GENERATOR TIMING

EXTENDED TIMEOUT FUNCTION

There are three timeouts associated with the COM 9026 operation.

Response Time

This timeout is equal to the round trip propagation delay between the 2 furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM 9026 to start sending a message in response to a received message) which is known to be 12 microseconds. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 31 microseconds translates to a distance of about 4 miles. The flow chart in figure 3 uses a value of 74.7 microseconds (31 + 31 + 12 + margin) to determine if any node will respond.

Idle Time

This time is associated with a NETWORK RECONFIGURATION. Refering to figure 3, during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. Every other node on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 78 microseconds. This 78 microsecond is equal to the response time of 74.7 microseconds plus the time it takes the COM 9026 to retransmit another message (usually another INVITATION TO TRANSMIT). The actual timeout is set to 78.2 microseconds to allow for margin.

Reconfiguration Time

If any node does not receive the token within this time, the node will initiate a NETWORK RECONFIGURATION.

The ET2 and ET1 inputs allow the network to operate over longer distances than the 4 miles stated earlier. DC levels on these inputs control the maximum distances over which the COM 9026 can operate by controlling the 3 timeout values described above. Table 1 illustrates the response time and reconfiguration time as a function of the ET2 and ET1 inputs. The idle time will always be equal to the response time plus 3.5 microseconds. It should be noted that for proper network operation, all COM 9026's connected to the same network must have the same response time, idle time and reconfiguration time.

ET2	ET1	RESPONSE TIME (μs)	RECONFIGURATION TIME (ms)
1	1	74.7	840
1	0	283.4	1680
0	1	561.8	1680
0	0	1118.6	1680

TABLE 1
COM 9026 INTERNAL PROGRAMMABLE TIMER VALUES

I/O COMMANDS

I/O commands are executed by activating the $\overline{IOREQ}$ input. The COM 9026 will interrogate the AD0 and the R/$\overline{W}$ inputs at the AS time to execute commands according to the following table:

$\overline{IOREQ}$	AD0	R/$\overline{W}$	FUNCTION
low	low	low	write interrupt mask
low	low	high	read status register
low	high	low	write COM 9026 command
low	high	high	reserved for future use

READ STATUS REGISTER

Execution of this command places the contents of the status register on the data bus (AD7-AD0) during the read portion of the processor's read cycle. The COM 9026 status register contents are defined as follows:

BIT 7—Receiver inhibited (RI)—This bit, if set high, indicates that a packet has been deposited into the RAM buffer page nn as specified by the last ENABLE RECEIVE TO PAGE nn command. The setting of this bit can cause an interrupt via INTR if enabled during a WRITE INTERRUPT MASK command. No messages will be received until an ENABLE RECEIVE TO PAGE nn command is issued. After any message is received, the receiver is automatically inhibited by setting this bit to a logic one.

BIT 6—Extended Timeout Status 2 (ETS2)—This bit reflects the current logic value tied to the ET2 input pin (pin 1).

BIT 5—Extended Timeout Status 1 (ETS1)—This bit reflects the current logic value tied to the ET1 input pin (pin 3).

Data Sheets

BIT 4—Power On Reset (POR)—This bit, if set high, indicates that the COM 9026 has received an active signal on the $\overline{POR}$ input (pin 40). The setting of this bit will cause a nonmaskable interrupt via INTR.

BIT 3—Test (TEST)—This bit is intended for test and diagnostic purposes. It will be a logic zero under any normal operating conditions.

BIT 2—Reconfiguration (RECON)—This bit, if set high, indicates that the reconfiguration timer has timed out because the RX input was idle for 78.2 microseconds. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command. The bit is reset low during a CLEAR FLAGS command.

BIT 1—Transmit Message Acknowledged (TMA)—This bit, if set high, indicates that the packet transmitted as a result of an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast mesages are never acknowledged.

BIT 0—Transmitter Available (TA)—This bit, if set high, indicates that the transmitter is available for transmitting. This bit is set at the conclusion of a ENABLE TRANSMIT FROM PAGE nn command or upon the execution of a DISABLE TRANSMITTER command. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command.

WRITE INTERRUPT MASK

The COM 9026 is capable of generating an interrupt signal when certain status bits become true. A write to the MASK register specifies which status bits can generate the interrupt. The bit positions in the MASK register are in the same position as their corresponding status bits in the STATUS register with a logic one in a bit position enabling the corresponding interrupt. The setting of the TMA, EST1, and EST2 status bits will never cause an interrupt. The POR status bit will cause a non-maskable interrupt regardless of the value of the corresponding MASK register bit. The MASK register takes on the following bit definition:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE INHIBIT	XXX	XXX	XXX	XXX	RECON TIMER	XXX	TRANSMITTER AVAILABLE

The three maskable status bits are anded with their respective mask bits, and the results, along with the POR status bit, are or'ed to produce the processor interrupt signal INTR. This signal returns to its inactive low state when the interrupting status bit is reset to a logic "0" or when the corresponding bit in the MASK register is reset to a logic "0". To clear an interrupt generated as a result of a Power On Reset or Reconfiguration occurance, the CLEAR FLAGS command should be used. To clear an interrupt generated as a result of a completed transmission (TA) or a completed reception (RI), the corresponding masks bits should be reset to a logic zero.

WRITE COM 9026 COMMANDS

Execution of the following commands are initiated by performing a processor I/O write with the written data defining the following commands:

WRITTEN DATA	COMMAND
00000000	reserved for future use
00000001	DISABLE TRANSMITTER—This command will cancel any pending transmit command (transmission has not yet started) when the COM 9026 next receives the token. This command will set the TA (Transmitter Available) status bit when the token is received.
00000010	DISABLE RECEIVER—This command will cancel any pending receive command. If the COM 9026 is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion.
000nn011	ENABLE TRANSMIT FROM PAGE nn—This command prepares the COM 9026 to begin a transmit sequence from RAM buffer page nn the next time it receives the token. When this command is loaded, the TA and TMA bits are set to a logic "0". The TA bit is set to a logic one upon completion of the transmit sequence. The TMA bit will have been set by this time if the COM 9026 has received an acknowledgement from the destination COM 9026. This acknowledgement is strictly hardware level which is sent by the receiving COM 9026 before its controlling processor is even aware of message reception. It is also possible for this acknowledgement to get lost due to line errors, etc. This implies that the TMA bit is not a guarantee of proper destination reception. Refer to figure 3 for details of the transmit sequence and its relation to the TA and TMA status bits.
b00nn100	ENABLE RECEIVE TO PAGE nn—This command allows the COM 9026 to receive data packets into RAM buffer page nn and sets the RI status bit to a logic zero. If "b" is a logic "1", the COM 9026 will also receive broadcast transmissions. A broadcast transmission is a transmission to ID zero. The RI status bit is set to a logic one upon successful reception of a message.
0000c101	DEFINE CONFIGURATION—If c is a logic "1", the COM 9026 will handle short as well as long packets. If c is a logic "0", the COM 9026 will only handle short packets (less than 254 bytes).
000rp110	CLEAR FLAGS—If p is a logic "1" the POR status flag is cleared. If r is a logic "1", the RECON status flag is cleared.

All other combinations of written data are not permitted and can result in incorrect chip and/or network operation.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0 to 70°C
Storage Temperature Range	-55 to 150°C
Lead Temperature (soldering, 10 seconds)	+325°C
Positive Voltage on any pin	+8V
Negative Voltage on any pin, with respect to ground	-0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH1}	Input high voltage 1	2.2		V_{CC}	V	except CA and CLK
V_{IH2}	Input high voltage 2	V_{CC}-0.5		6.5	V	for CA or CLK
V_{OL1}	output low voltage 1			0.4	V	I_{OL} = 1.6 ma
V_{OL2}	output low voltage 2			0.5	V	I_{OL} = 2.0 ma
V_{OH}	output high voltage (1)	2.4			V	
I_L	input leakage current			±10	µA	
C_{IN}	input capacitance			20	pf	
C_{DB}	data bus capacitance			50	pf	
C_L	all other capacitance			30	pf	
I_{CC}	power supply current			350	ma	

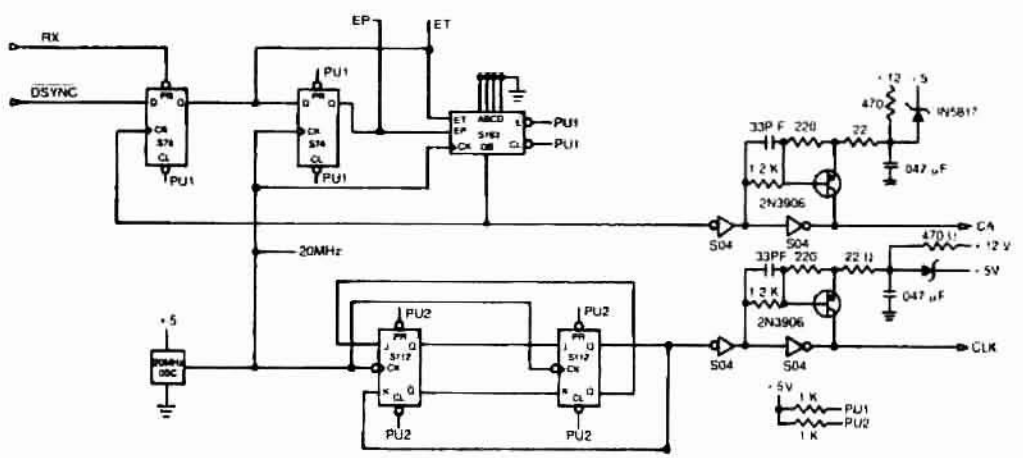


FIGURE 20—TYPICAL CLOCK GENERATOR CIRCUITRY

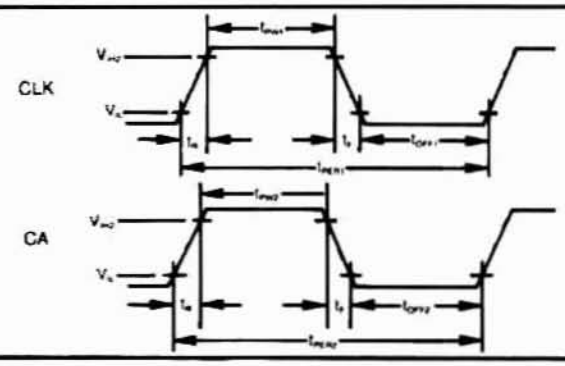
Data Sheets

AC ELECTRICAL CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5.0V ± 5%)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
t_{PW1}	CLK pulse width	65			ns	
t_{PER1}	CLK period	190	200	600	ns	
t_{OFF1}	CLK off time	65			ns	
t_{PW2}	CA pulse width	60			ns	
t_{PER2}	CA period	190			ns	
t_{OFF2}	CA off time	60	100	300	ns	
t_R	CLK, CA rise time			20	ns	
t_F	CLK, CA fall time			20	ns	
t_1	width of addr. strobe	50			ns	
t_2	REQ output delay	0		100	ns	
t_3	WAIT assertion delay	0		200	ns	
t_4	delay to rising edge of processor cycle	t_5		$2t_5 + 100$	ns	$t_5 = t_{PER1}$
t_5	data hold into COM 9026	80			ns	
t_6	setup COM 9026 data out	60			ns	
t_7	$\overline{WE}$ delay from CLK	0		100	ns	
t_8	$\overline{TX}$ on delay from CA falling edge	10		150	ns	
t_9	$\overline{TX}$ off delay from CA rising edge	10		150	ns	
t_{10}	AS period	7/2 t_5			ns	$t_5 = t_{PER1}$
t_{11}	$\overline{DSYNC}$ delay from CA rising edge	10		150	ns	
t_{12}	delay to wait off	20		100	ns	
t_{13}	$\overline{DWR}$ setup time	50			ns	
t_{14}	$\overline{ILE}$ delay from CLK	10		100	ns	
t_{15}	processor addr. setup from $\overline{ADIE}$,			50	ns	
t_{16}	processor command setup time	125			ns	
t_{17}	addr. enable setup time to $\overline{L}$	50			ns	
t_{18}	addr. hold time from $\overline{L}$	50			ns	
t_{19}	strobe and data hold for read	20			ns	
t_{20}	AD bus HI impedance to $\overline{OE}$s	0			ns	
t_{21}	delay of $\overline{IDLD}$ from CLK rising edge	0		120	ns	
t_{22}	delay of IDDAT from CLK rising edge	0		50	ns	
t_{23}	off delay from CLK rising edge	0		100	ns	
t_{24}	addr. to RAM data valid			300	ns	
t_{25}	$\overline{OE}$ setup to WAIT falling edge	140			ns	
t_{26}	strobe & data hold for write	50			ns	
t_{27}	addr. enable setup to WAIT	300			ns	
t_{28}	$\overline{ADIE}$ to $\overline{OE}$ delay	40			ns	
t_{29}	COM 9026 write data hold time	80			ns	
t_{30}	$\overline{OE}$ to RAM data valid	0		140	ns	
t_{31}	status setup to AS falling edge	50			ns	
t_{32}	status hold from AS falling edge	50			ns	
t_{33}	RX setup to CA rising edge	80			ns	
t_{34}	RX hold time from CA rising edge	30			ns	
t_{35}	$\overline{POR}$ active time	100			ms	after V_{cc} has been stable for time t_{35}, the minimum $\overline{POR}$ active time is 10 cycles of CLK.

The above timing information is valid for a worst case 40% to 60% duty cycle on CLK. All times are measured from the 50% point of the signals.

FIGURE 10— CLK, CA AC CHARACTERISTICS



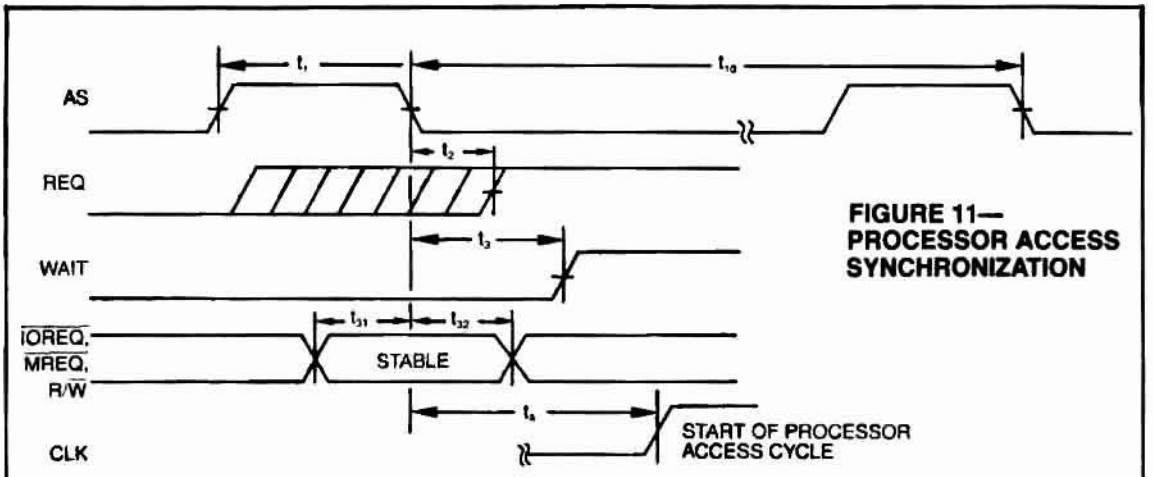


FIGURE 11—PROCESSOR ACCESS SYNCHRONIZATION

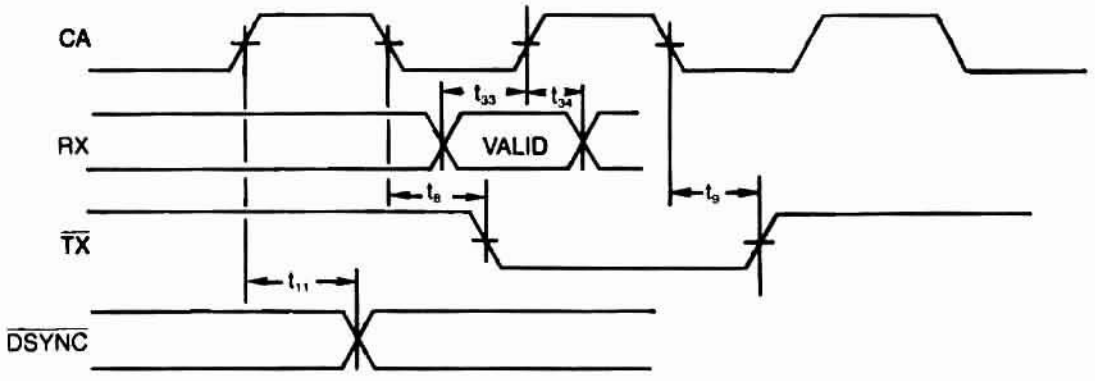


FIGURE 12—TRANSMIT AND RECEIVE TIMING

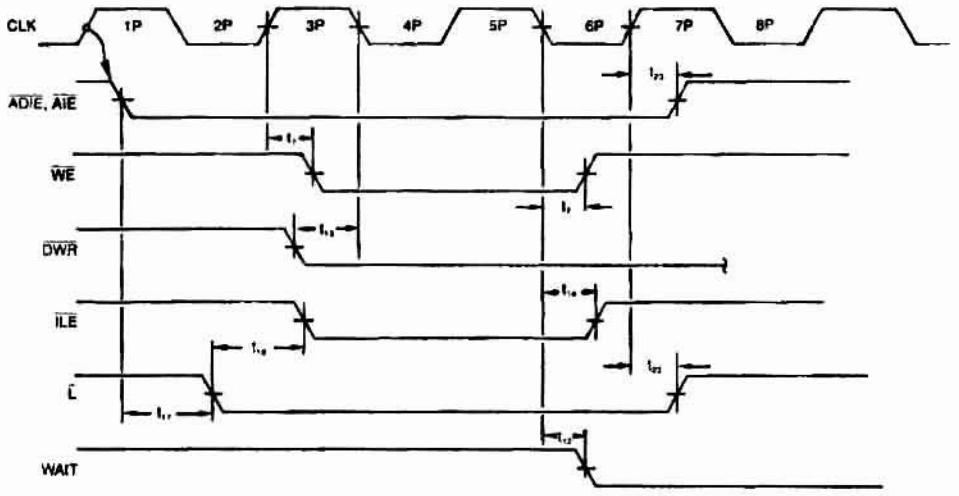


FIGURE 13—PROCESSOR WRITE RAM AC TIMING

Data Sheets

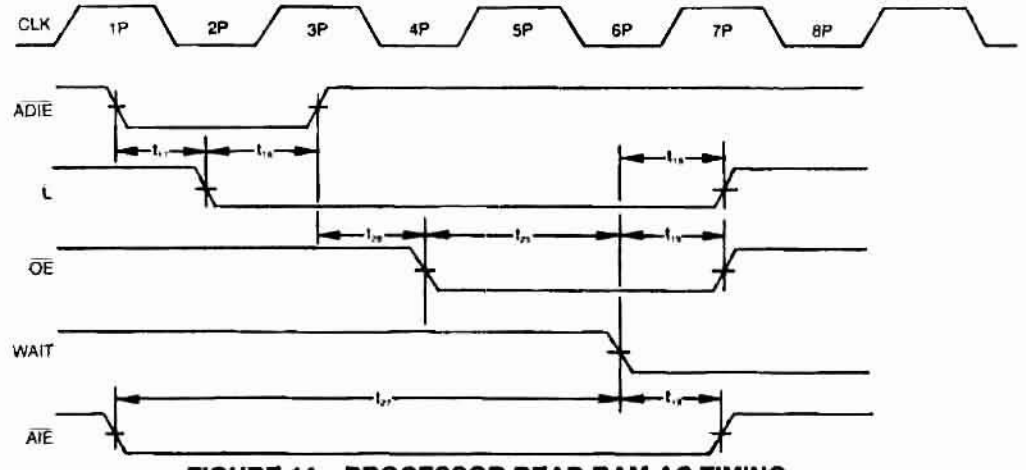


FIGURE 14—PROCESSOR READ RAM AC TIMING

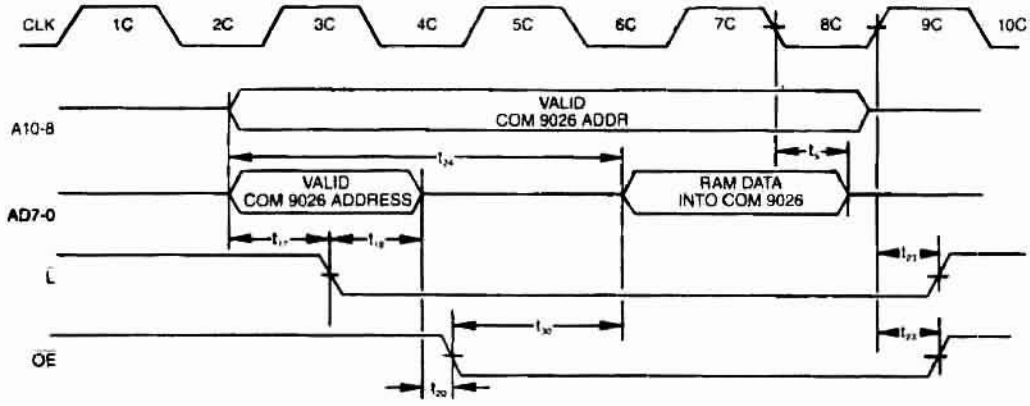


FIGURE 15—COM 9026 READ RAM AC TIMING

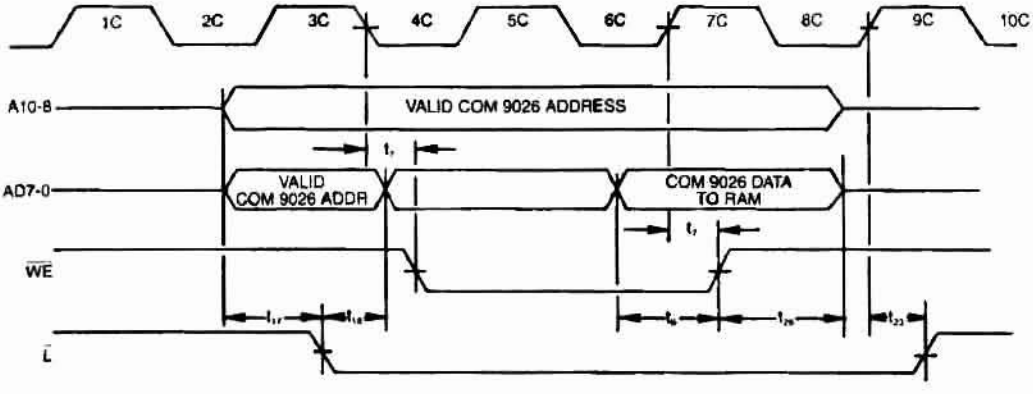


FIGURE 16—COM 9026 WRITE RAM AC TIMING

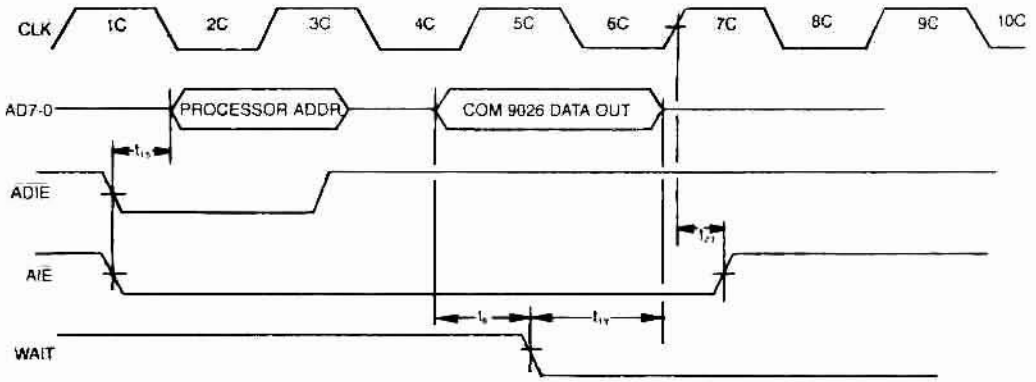


FIGURE 17—PROCESSOR READ COM 9026 AC TIMING

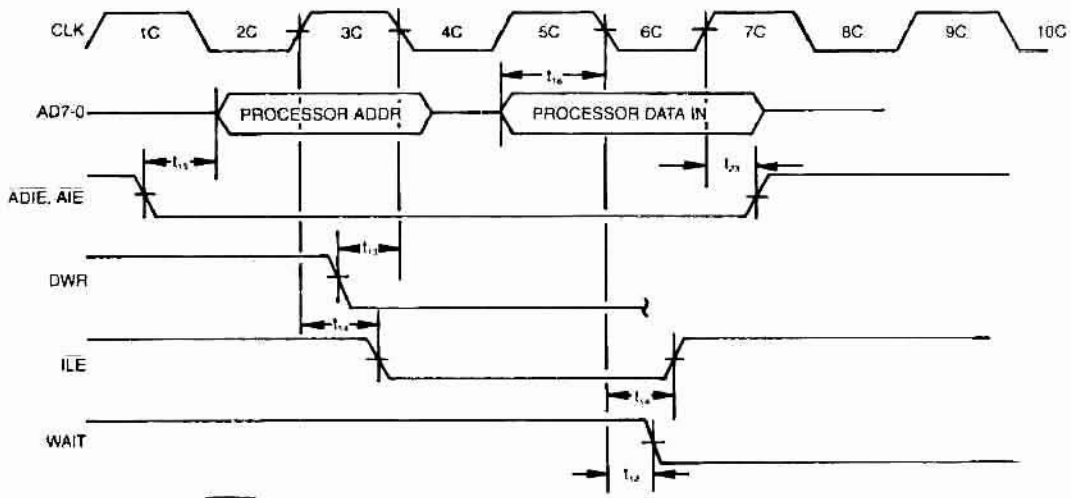


FIGURE 18—PROCESSOR WRITE COM 9026 AC TIMING

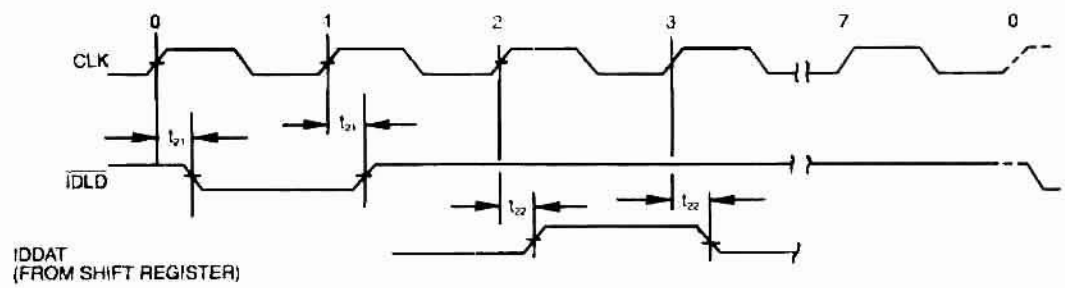


FIGURE 19—ID INPUT AC TIMING

STANDARD MICROSYSTEMS CORPORATION

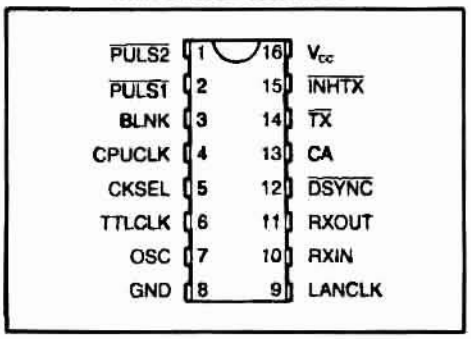
COM 9032

COM 9032
Local Area Network Transceiver
LANT

FEATURES

- ☐ Reduces chip count for COM 9026 ARCNET* implementations by 6-8 TTL chips
- ☐ Performs all clock generation functions for the COM 9026
- ☐ Compatible with the COM 9026
- ☐ Provides line drive signals for transmission
- ☐ Converts incoming serial receive data to NRZ data format
- ☐ Generates two 4 MHz general purpose clocks

PIN CONFIGURATION



GENERAL DESCRIPTION

The COM 9032 local area network transceiver is a companion chip to the COM 9026 Local Area Network Controller (LANC) and will perform the additional functions necessary to allow simple interface to a transmission media for all ARCNET* (or equivalent) local area networks. Using a 20 MHz input clock, the COM 9032 will produce two, 5 MHz clocks for the COM 9026. The first 5 MHz clock is free running and will directly feed the CLK input of the COM 9026 (pin 19). The second 5 MHz clock has start/stop capability which is controlled by the DSYNC output of the COM 9026 (pin 36) and the received data input as required by the COM 9026 (pin 2). Two additional 4 MHz free running clocks are also generated on the COM 9032 to allow operation of other logic, a microprocessor, or an LSI controller.

During data reception, the COM 9032 will convert incoming serial receive data from the transmission media to NRZ form which will directly feed the RX input of the COM 9026 (pin 38). During transmission, the COM 9032 converts the transmit data from the COM 9026 (TX, pin 37) into the waveforms necessary to drive opposite ends of the rf transformer used in the ARCNET* cable electronics shown in figure 2.

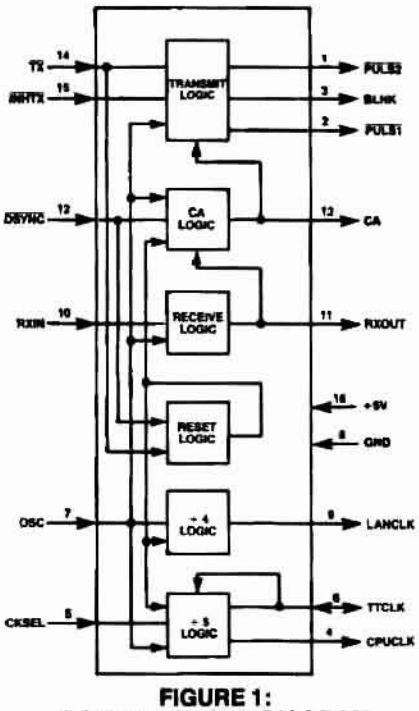


FIGURE 1:
COM 9032 BLOCK DIAGRAM

*ARCNET is a registered trademark of the Datapoint Corporation.

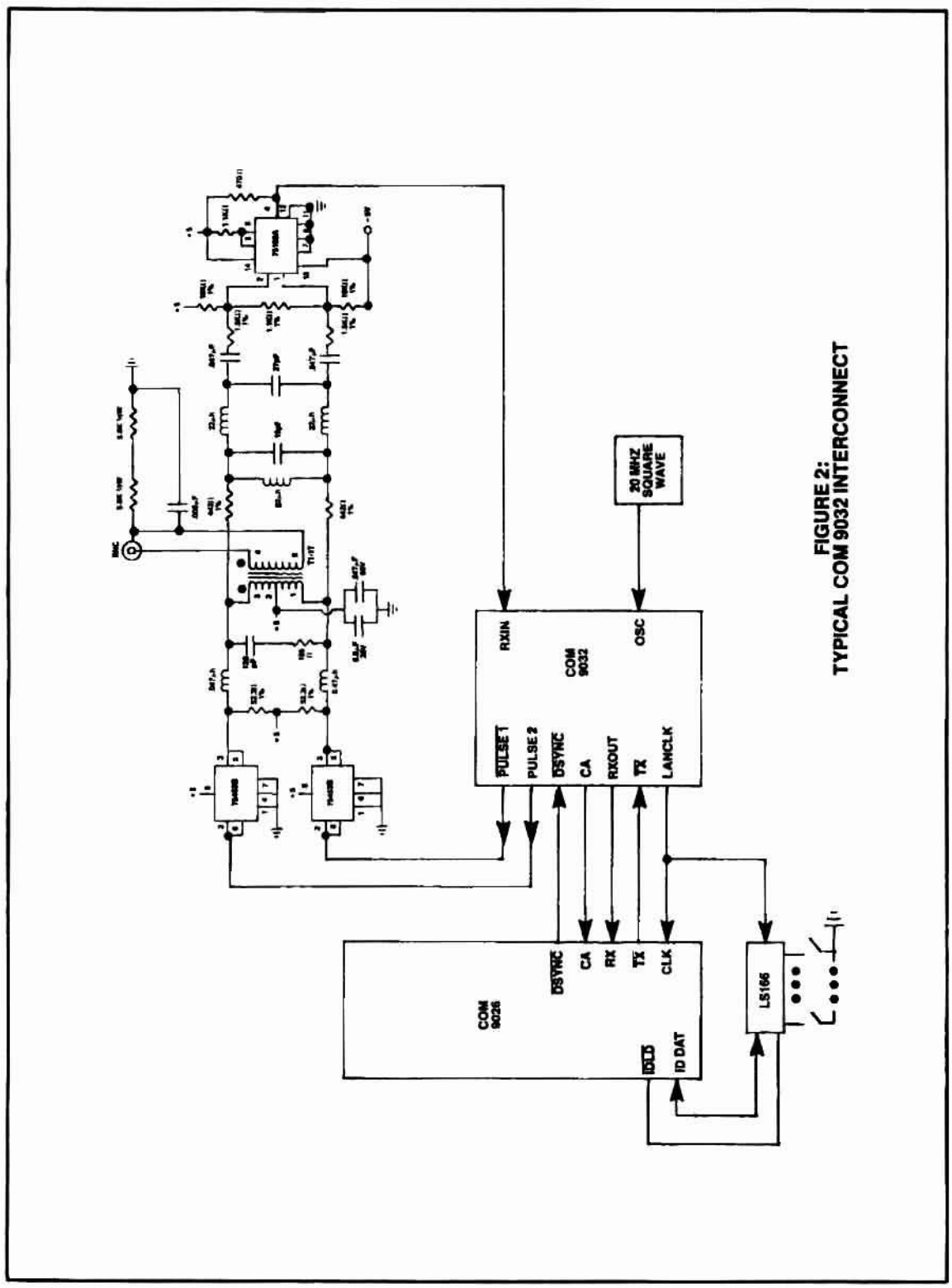


FIGURE 2:
TYPICAL COM 9032 INTERCONNECT

Data Sheets

DESCRIPTION OF PIN FUNCTIONS

(Refer to figure 2)

COM 9026 INTERFACE

PIN NO.	NAME	SYMBOL	FUNCTION
1, 2	PULSE 2 PULSE 1	$\overline{PULS2}$ $\overline{PULS1}$	$\overline{PULS2}$ and $\overline{PULS1}$ are two nonoverlapping negative pulses which occur every time the $\overline{TX}$ input is pulsed. $\overline{PULS2}$ and $\overline{PULS1}$ are used to feed an external driver as shown in figure 2.
3	BLANK	$\overline{BLNK}$	When used with the circuitry shown in figure 2, this output should be left unconnected. The timing of this signal is shown in figure 4.
10	RECEIVE IN	RXIN	This input is the recovered receive data from the network. For each dipulse appearing on the network, the comparator shown in figure 2 will produce a positive pulse which directly feeds this input.
11	RECEIVE OUT	RXOUT	This output is the NRZ data generated as a function of the RXIN pulse waveform which directly feeds the RX input of the COM 9026 (pin 38).
12	DELAYED SYNC	$\overline{DSYNC}$	This active low input, which is asserted by the COM 9026, will halt the CA clock output.
13	CA	$\overline{CA}$	This output is a 5 MHz start/stop clock that is halted when $\overline{DSYNC}$ goes active low and restarted by a low signal on the RXOUT output. This clock is capable of driving 70 pf plus one LS load with 20 nanoseconds rise and fall times.
14	TRANSMIT DATA	$\overline{TX}$	This input, which is asserted by the COM 9026, is the serial data transmitted by the node.
15	TRANSMIT INHIBIT	$\overline{INHTX}$	This active low input inhibits the $\overline{TX}$ signal from initiating transmit signals by forcing $\overline{PULS1}$ and $\overline{PULS2}$ to a high and $\overline{BLNK}$ to a low. This signal should be asserted during a power on reset condition.

SYSTEM CLOCK INTERFACE

PIN NO.	NAME	SYMBOL	FUNCTION
4	CPU CLOCK	CPUCLK	This output is a 4 MHz free running clock capable of driving 130 pf with 30 nanosecond rise and fall times. It is identical to the TTLCLK input when CKSEL is high. When CKSEL is low, this output becomes the inversion of the signal that is fed into the TTLCLK input.
5	CLOCK SELECT	CKSEL	This input selects the clock interface option for the TTLCLK and CPUCLK. When this signal is high, both the TTLCLK and CPUCLK are identical 4 MHz free running clock outputs which are generated from the 20 MHz input clock (OSC) via a divide by 5 frequency divider. When this input is low, the TTLCLK pin becomes an input and the CPUCLK output will produce the inversion of the signal appearing on TTLCLK input.
6	TTL CLOCK	TTLCLK	This pin can be either an input or an output depending on the state of the CKSEL input. When CKSEL is high, a free running 4 MHz clock is ouput. When CKSEL is low, the pin becomes an input which drives an inverter that feeds the CPUCLK output.
7	OSCILLATOR	OSC	This input requires a 20 MHz clock.
9	LOCAL AREA NETWORK CLOCK	LANCLK	This output will supply the free running 5 MHz clock to the COM 9026, pin 19. It is capable of driving 70 pf plus one LS load with 20 nanoseconds rise and fall times.
8	GROUND	GND	Ground
16	+5 VOLT SUPPLY	V_{CC}	Power Supply

FUNCTIONAL DESCRIPTION

Transmit logic (refer to figures 2 and 4)

The COM 9026, when transmitting data on $\overline{TX}$, will produce a negative pulse of 200 nanoseconds in duration to indicate a logic "1" and no pulse to indicate a logic "0". Refering to figure 4, a 200 nanosecond pulse on $\overline{TX}$ is converted to two, 100 nanosecond nonoverlapping pulses shown as $\overline{PULS1}$ and $\overline{PULS2}$. The signals $\overline{PULS1}$ and $\overline{PULS2}$ are used to create a 200 nanosecond wide dipulse by driving opposite ends of the RF transformer shown in gure 2.

Receive logic (refer to figures 2 and 5)

As each dipulse appears on the cable, it is coupled through the RF transformer, passes through the matched filter, and feeds the 75108B comparator. The 75108B produces a positive pulse for each dipulse received from the cable. These pulses are captured by the COM 9032 and are converted to NRZ data with the NRZ data bit boundaries being delayed by 5 OSC clock periods as shown in figure 5. As each byte is received by the COM 9026, the CA clock is stopped by the COM 9026 (via $\overline{DSYNC}$) until the first bit of the next byte is received which will automatically restart the CA clock. The COM 9026 uses the CA clock to sample the NRZ data and these sample points are shown in figure 5.

Typically, RXIN pulses occur at multiples of the transmission rate of 2.5 MHz (400 nanoseconds). The COM 9032 can tolerate distortion of plus or minus 100 nanoseconds and still correctly capture and convert the RXIN pulses to NRZ format.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −55° to 150°C
Lead Temperature (soldering, 10 sec.) ..... 325°C
Positive Voltage on any Pin ..... +8V
Negative Voltage on any Pin ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
INPUT VOLTAGES					
V_{IH}	2.0			V	
V_{IL}			0.8	V	
OUTPUT VOLTAGES					
V_{OH1}	4.0			V	I_{OH} = −0.4 mA, $\overline{PULS1}$, $\overline{PULS2}$, RXOUT and TTLCLK outputs.
V_{OL1}			0.4	V	I_{OH} = 4.0 mA, PULS1, PULS2, RXOUT and TTLCLK outputs.
V_{OH2}	V_{CC}-0.5			V	I_{OH} = −0.1 mA, CPUCLK output.
V_{OL2}			0.4	V	I_{OL} = 0.1 mA, CPUCLK output.
V_{OH3}	V_{CC}-0.5			V	I_{OH} = −0.1 mA, CA and LANCLK outputs.
V_{OL3}			0.4	V	I_{OL} = 0.4 mA, CA and LANCLK outputs.
LEAKAGE CURRENT					
I_{I1}			50	µA	TTLCLK input with CKSEL low.
I_{I2}			10	µA	all other inputs.
INPUT CAPACITANCE					
C_{IN}			30	pf	
SUPPLY CURRENT					
I_{CC}			20	mA	at 20 MHz OSC frequency.

AC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
OSC Input					
t_{CY1}		50		ns	
t_{CH1}	20			ns	
t_{CL1}	20			ns	
CA, LANCLK					
t_{CY2}		200		ns	
t_{CH2}	75			ns	
t_{CL2}	75			ns	
t_{F2}			20	ns	
t_{R2}			20	ns	
TTLCLK					
t_{CY3}		250		ns	
t_{CH3}	110			ns	
t_{CL3}	110			ns	
CPUCLK (CKSEL is high)					
t_{CY4}		250		ns	
t_{CH4}	110			ns	
t_{CL4}	110			ns	
t_{F4}			30	ns	
t_{R4}			30	ns	
t_{DCK}			45	ns	for CKSEL low.
TRANSMIT TIMING					
t_{STC}		10		ns	
t_{STO}	10			ns	
t_{HTC}		10		ns	
t_{HTO}	10			ns	
t_{FXC}	60			ns	
t_{FXD}			60	ns	
t_{DP}			60	ns	
t_{PTW}		$2t_{CY1}$		ns	
t_{WB}		t_{CY1}		ns	
t_{PZW}		$2t_{CY1}$		ns	
t_{RST}			40	ns	
RECEIVE TIMING					
t_{RS}	10			ns	
t_{RW}	10			ns	
t_{DD}			70	ns	
t_{RD}		$5t_{CY1} + t_{DD}$		ns	
t_{SSD}	10			ns	
t_{SSC}		20		ns	
t_{RDW}		400		ns	

Data Sheets

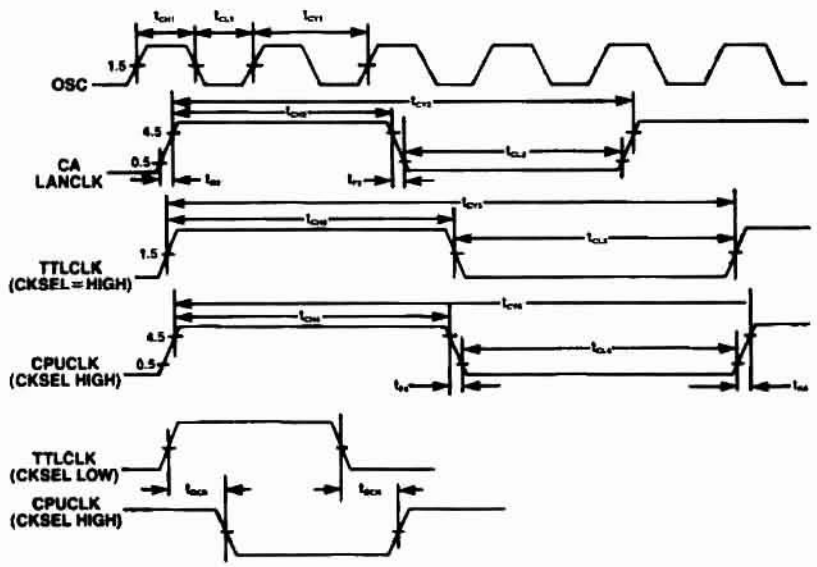


FIGURE 3: CLOCK TIMING

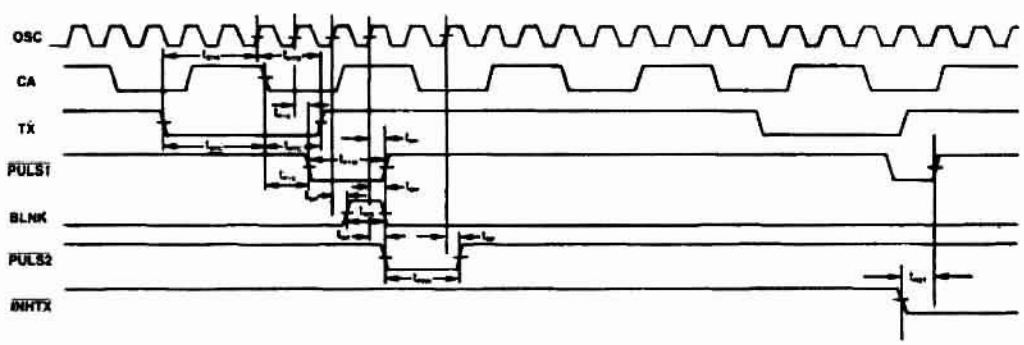


FIGURE 4: TRANSMIT TIMING PARAMETERS

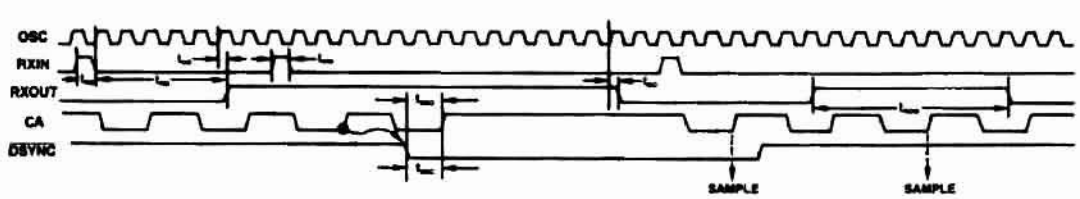


FIGURE 5: RECEIVE TIMING PARAMETERS

STANDARD MICROSYSTEMS CORPORATION

4/83-5M

Appendix A
ID Node Number Lookup Table

ID NO.		POSITION							
DEC	HEX	0	1	2	3	4	5	6	7
1	1	ON	ON	ON	ON	ON	ON	ON	OFF
2	2	ON	ON	ON	ON	ON	ON	OFF	ON
3	3	ON	ON	ON	ON	ON	ON	OFF	OFF
4	4	ON	ON	ON	ON	ON	OFF	ON	ON
5	5	ON	ON	ON	ON	ON	OFF	ON	OFF
6	6	ON	ON	ON	ON	ON	OFF	OFF	ON
7	7	ON	ON	ON	ON	ON	OFF	OFF	OFF
8	8	ON	ON	ON	ON	OFF	ON	ON	ON
9	9	ON	ON	ON	ON	OFF	ON	ON	OFF
10	A	ON	ON	ON	ON	OFF	ON	OFF	ON
11	B	ON	ON	ON	ON	OFF	ON	OFF	OFF
12	C	ON	ON	ON	ON	OFF	OFF	ON	ON
13	D	ON	ON	ON	ON	OFF	OFF	ON	OFF
14	E	ON	ON	ON	ON	OFF	OFF	OFF	ON
15	F	ON	ON	ON	ON	OFF	OFF	OFF	OFF
16	10	ON	ON	ON	OFF	ON	ON	ON	ON
17	11	ON	ON	ON	OFF	ON	ON	ON	OFF
18	12	ON	ON	ON	OFF	ON	ON	OFF	ON
19	13	ON	ON	ON	OFF	ON	ON	OFF	OFF
20	14	ON	ON	ON	OFF	ON	OFF	ON	ON
21	15	ON	ON	ON	OFF	ON	OFF	ON	OFF
22	16	ON	ON	ON	OFF	ON	OFF	OFF	ON
23	17	ON	ON	ON	OFF	ON	OFF	OFF	OFF
24	18	ON	ON	ON	OFF	OFF	ON	ON	ON
25	19	ON	ON	ON	OFF	OFF	ON	ON	OFF
26	1A	ON	ON	ON	OFF	OFF	ON	OFF	ON
27	1B	ON	ON	ON	OFF	OFF	ON	OFF	OFF
28	1C	ON	ON	ON	OFF	OFF	OFF	ON	ON
29	1D	ON	ON	ON	OFF	OFF	OFF	ON	OFF
30	1E	ON	ON	ON	OFF	OFF	OFF	OFF	ON
31	1F	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
32	20	ON	ON	OFF	ON	ON	ON	ON	ON
33	21	ON	ON	OFF	ON	ON	ON	ON	OFF
34	22	ON	ON	OFF	ON	ON	ON	OFF	ON
35	23	ON	ON	OFF	ON	ON	ON	OFF	OFF
36	24	ON	ON	OFF	ON	ON	OFF	ON	ON

ID Node Number Lookup Table

ID NO.		POSITION							
DEC	HEX	0	1	2	3	4	5	6	7
37	25	ON	ON	OFF	ON	ON	OFF	ON	OFF
38	26	ON	ON	OFF	ON	ON	OFF	OFF	ON
39	27	ON	ON	OFF	ON	ON	OFF	OFF	OFF
40	28	ON	ON	OFF	ON	OFF	ON	ON	ON
41	29	ON	ON	OFF	ON	OFF	ON	ON	OFF
42	2A	ON	ON	OFF	ON	OFF	ON	OFF	ON
43	2B	ON	ON	OFF	ON	OFF	ON	OFF	OFF
44	2C	ON	ON	OFF	ON	OFF	OFF	ON	ON
45	2D	ON	ON	OFF	ON	OFF	OFF	ON	OFF
46	2E	ON	ON	OFF	ON	OFF	OFF	OFF	ON
47	2F	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
48	30	ON	ON	OFF	OFF	ON	ON	ON	ON
49	31	ON	ON	OFF	OFF	ON	ON	ON	OFF
50	32	ON	ON	OFF	OFF	ON	ON	OFF	ON
51	33	ON	ON	OFF	OFF	ON	ON	OFF	OFF
52	34	ON	ON	OFF	OFF	ON	OFF	ON	ON
53	35	ON	ON	OFF	OFF	ON	OFF	ON	OFF
54	36	ON	ON	OFF	OFF	ON	OFF	OFF	ON
55	37	ON	ON	OFF	OFF	ON	OFF	OFF	OFF
56	38	ON	ON	OFF	OFF	OFF	ON	ON	ON
57	39	ON	ON	OFF	OFF	OFF	ON	ON	OFF
58	3A	ON	ON	OFF	OFF	OFF	ON	OFF	ON
59	3B	ON	ON	OFF	OFF	OFF	ON	OFF	OFF
60	3C	ON	ON	OFF	OFF	OFF	OFF	ON	ON
61	3D	ON	ON	OFF	OFF	OFF	OFF	ON	OFF
62	3E	ON	ON	OFF	OFF	OFF	OFF	OFF	ON
63	3F	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
64	40	ON	OFF	ON	ON	ON	ON	ON	ON
65	41	ON	OFF	ON	ON	ON	ON	ON	OFF
66	42	ON	OFF	ON	ON	ON	ON	OFF	ON
67	43	ON	OFF	ON	ON	ON	ON	OFF	OFF
68	44	ON	OFF	ON	ON	ON	OFF	ON	ON
69	45	ON	OFF	ON	ON	ON	OFF	ON	OFF
70	46	ON	OFF	ON	ON	ON	OFF	OFF	ON
71	47	ON	OFF	ON	ON	ON	OFF	OFF	OFF
72	48	ON	OFF	ON	ON	OFF	ON	ON	ON

ID Node Number Lookup Table

ID NO.		POSITION							
DEC	HEX	0	1	2	3	4	5	6	7
73	49	ON	OFF	ON	ON	OFF	ON	ON	OFF
74	4A	ON	OFF	ON	ON	OFF	ON	OFF	ON
75	4B	ON	OFF	ON	ON	OFF	ON	OFF	OFF
76	4C	ON	OFF	ON	ON	OFF	OFF	ON	ON
77	4D	ON	OFF	ON	ON	OFF	OFF	ON	OFF
78	4E	ON	OFF	ON	ON	OFF	OFF	OFF	ON
79	4F	ON	OFF	ON	ON	OFF	OFF	OFF	OFF
80	50	ON	OFF	ON	OFF	ON	ON	ON	ON
81	51	ON	OFF	ON	OFF	ON	ON	ON	OFF
82	52	ON	OFF	ON	OFF	ON	ON	OFF	ON
83	53	ON	OFF	ON	OFF	ON	ON	OFF	OFF
84	54	ON	OFF	ON	OFF	ON	OFF	ON	ON
85	55	ON	OFF	ON	OFF	ON	OFF	ON	OFF
86	56	ON	OFF	ON	OFF	ON	OFF	OFF	ON
87	57	ON	OFF	ON	OFF	ON	OFF	OFF	OFF
88	58	ON	OFF	ON	OFF	OFF	ON	ON	ON
89	59	ON	OFF	ON	OFF	OFF	ON	ON	OFF
90	5A	ON	OFF	ON	OFF	OFF	ON	OFF	ON
91	5B	ON	OFF	ON	OFF	OFF	ON	OFF	OFF
92	5C	ON	OFF	ON	OFF	OFF	OFF	ON	ON
93	5D	ON	OFF	ON	OFF	OFF	OFF	ON	OFF
94	5E	ON	OFF	ON	OFF	OFF	OFF	OFF	ON
95	5F	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF
96	60	ON	OFF	OFF	ON	ON	ON	ON	ON
97	61	ON	OFF	OFF	ON	ON	ON	ON	OFF
98	62	ON	OFF	OFF	ON	ON	ON	OFF	ON
99	63	ON	OFF	OFF	ON	ON	ON	OFF	OFF
100	64	ON	OFF	OFF	ON	ON	OFF	ON	ON
101	65	ON	OFF	OFF	ON	ON	OFF	ON	OFF
102	66	ON	OFF	OFF	ON	ON	OFF	OFF	ON
103	67	ON	OFF	OFF	ON	ON	OFF	OFF	OFF
104	68	ON	OFF	OFF	ON	OFF	ON	ON	ON
105	69	ON	OFF	OFF	ON	OFF	ON	ON	OFF
106	6A	ON	OFF	OFF	ON	OFF	ON	OFF	ON
107	6B	ON	OFF	OFF	ON	OFF	ON	OFF	OFF
108	6C	ON	OFF	OFF	ON	OFF	OFF	ON	ON

ID Node Number Lookup Table

ID NO. DEC	ID NO. HEX	POSITION 0	1	2	3	4	5	6	7
109	6D	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
110	6E	ON	OFF	OFF	ON	OFF	OFF	OFF	ON
111	6F	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
112	70	ON	OFF	OFF	OFF	ON	ON	ON	ON
113	71	ON	OFF	OFF	OFF	ON	ON	ON	OFF
114	72	ON	OFF	OFF	OFF	ON	ON	OFF	ON
115	73	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
116	74	ON	OFF	OFF	OFF	ON	OFF	ON	ON
117	75	ON	OFF	OFF	OFF	ON	OFF	ON	OFF
118	76	ON	OFF	OFF	OFF	ON	OFF	OFF	ON
119	77	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
120	78	ON	OFF	OFF	OFF	OFF	ON	ON	ON
121	79	ON	OFF	OFF	OFF	OFF	ON	ON	OFF
122	7A	ON	OFF	OFF	OFF	OFF	ON	OFF	ON
123	7B	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
124	7C	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
125	7D	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF
126	7E	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON
127	7F	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
128	80	OFF	ON	ON	ON	ON	ON	ON	ON
129	81	OFF	ON	ON	ON	ON	ON	ON	OFF
130	82	OFF	ON	ON	ON	ON	ON	OFF	ON
131	83	OFF	ON	ON	ON	ON	ON	OFF	OFF
132	84	OFF	ON	ON	ON	ON	OFF	ON	ON
133	85	OFF	ON	ON	ON	ON	OFF	ON	OFF
134	86	OFF	ON	ON	ON	ON	OFF	OFF	ON
135	87	OFF	ON	ON	ON	ON	OFF	OFF	OFF
136	88	OFF	ON	ON	ON	OFF	ON	ON	ON
137	89	OFF	ON	ON	ON	OFF	ON	ON	OFF
138	8A	OFF	ON	ON	ON	OFF	ON	OFF	ON
139	8B	OFF	ON	ON	ON	OFF	ON	OFF	OFF
140	8C	OFF	ON	ON	ON	OFF	OFF	ON	ON
141	8D	OFF	ON	ON	ON	OFF	OFF	ON	OFF
142	8E	OFF	ON	ON	ON	OFF	OFF	OFF	ON
143	8F	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
144	90	OFF	ON	ON	OFF	ON	ON	ON	ON

ID Node Number Lookup Table

ID NO.		POSITION							
DEC	HEX	0	1	2	3	4	5	6	7
145	91	OFF	ON	ON	OFF	ON	ON	ON	OFF
146	92	OFF	ON	ON	OFF	ON	ON	OFF	ON
147	93	OFF	ON	ON	OFF	ON	ON	OFF	OFF
148	94	OFF	ON	ON	OFF	ON	OFF	ON	ON
149	95	OFF	ON	ON	OFF	ON	OFF	ON	OFF
150	96	OFF	ON	ON	OFF	ON	OFF	OFF	ON
151	97	OFF	ON	ON	OFF	ON	OFF	OFF	OFF
152	98	OFF	ON	ON	OFF	OFF	ON	ON	ON
153	99	OFF	ON	ON	OFF	OFF	ON	ON	OFF
154	9A	OFF	ON	ON	OFF	OFF	ON	OFF	ON
155	9B	OFF	ON	ON	OFF	OFF	ON	OFF	OFF
156	9C	OFF	ON	ON	OFF	OFF	OFF	ON	ON
157	9D	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
158	9E	OFF	ON	ON	OFF	OFF	OFF	OFF	ON
159	9F	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
160	A0	OFF	ON	OFF	ON	ON	ON	ON	ON
161	A1	OFF	ON	OFF	ON	ON	ON	ON	OFF
162	A2	OFF	ON	OFF	ON	ON	ON	OFF	ON
163	A3	OFF	ON	OFF	ON	ON	ON	OFF	OFF
164	A4	OFF	ON	OFF	ON	ON	OFF	ON	ON
165	A5	OFF	ON	OFF	ON	ON	OFF	ON	OFF
166	A6	OFF	ON	OFF	ON	ON	OFF	OFF	ON
167	A7	OFF	ON	OFF	ON	ON	OFF	OFF	OFF
168	A8	OFF	ON	OFF	ON	OFF	ON	ON	ON
169	A9	OFF	ON	OFF	ON	OFF	ON	ON	OFF
170	AA	OFF	ON	OFF	ON	OFF	ON	OFF	ON
171	AB	OFF	ON	OFF	ON	OFF	ON	OFF	OFF
172	AC	OFF	ON	OFF	ON	OFF	OFF	ON	ON
173	AD	OFF	ON	OFF	ON	OFF	OFF	ON	OFF
174	AE	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
175	AF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
176	B0	OFF	ON	OFF	OFF	ON	ON	ON	ON
177	B1	OFF	ON	OFF	OFF	ON	ON	ON	OFF
178	B2	OFF	ON	OFF	OFF	ON	ON	OFF	ON
179	B3	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
180	B4	OFF	ON	OFF	OFF	ON	OFF	ON	ON

ID Node Number Lookup Table

ID NO.		POSITION							
DEC	HEX	0	1	2	3	4	5	6	7
181	B5	OFF	ON	OFF	OFF	ON	OFF	ON	OFF
182	B6	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
183	B7	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF
184	B8	OFF	ON	OFF	OFF	OFF	ON	ON	ON
185	B9	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
186	BA	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
187	BB	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
188	BC	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
189	BD	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
190	BE	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON
191	BF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
192	C0	OFF	OFF	ON	ON	ON	ON	ON	ON
193	C1	OFF	OFF	ON	ON	ON	ON	ON	OFF
194	C2	OFF	OFF	ON	ON	ON	ON	OFF	ON
195	C3	OFF	OFF	ON	ON	ON	ON	OFF	OFF
196	C4	OFF	OFF	ON	ON	ON	OFF	ON	ON
197	C5	OFF	OFF	ON	ON	ON	OFF	ON	OFF
198	C6	OFF	OFF	ON	ON	ON	OFF	OFF	ON
199	C7	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
200	C8	OFF	OFF	ON	ON	OFF	ON	ON	ON
201	C9	OFF	OFF	ON	ON	OFF	ON	ON	OFF
202	CA	OFF	OFF	ON	ON	OFF	ON	OFF	ON
203	CB	OFF	OFF	ON	ON	OFF	ON	OFF	OFF
204	CC	OFF	OFF	ON	ON	OFF	OFF	ON	ON
205	CD	OFF	OFF	ON	ON	OFF	OFF	ON	OFF
206	CE	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
207	CF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
208	D0	OFF	OFF	ON	OFF	ON	ON	ON	ON
209	D1	OFF	OFF	ON	OFF	ON	ON	ON	OFF
210	D2	OFF	OFF	ON	OFF	ON	ON	OFF	ON
211	D3	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
212	D4	OFF	OFF	ON	OFF	ON	OFF	ON	ON
213	D5	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
214	D6	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
215	D7	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF
216	D8	OFF	OFF	ON	OFF	OFF	ON	ON	ON

ID Node Number Lookup Table

ID NO. DEC	ID NO. HEX	POSITION 0	1	2	3	4	5	6	7
217	D9	OFF	OFF	ON	OFF	OFF	ON	ON	OFF
218	DA	OFF	OFF	ON	OFF	OFF	ON	OFF	ON
219	DB	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
220	DC	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
221	DD	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
222	DE	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON
223	DF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
224	E0	OFF	OFF	OFF	ON	ON	ON	ON	ON
225	E1	OFF	OFF	OFF	ON	ON	ON	ON	OFF
226	E2	OFF	OFF	OFF	ON	ON	ON	OFF	ON
227	E3	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
228	E4	OFF	OFF	OFF	ON	ON	OFF	ON	ON
229	E5	OFF	OFF	OFF	ON	ON	OFF	ON	OFF
230	E6	OFF	OFF	OFF	ON	ON	OFF	OFF	ON
231	E7	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
232	E8	OFF	OFF	OFF	ON	OFF	ON	ON	ON
233	E9	OFF	OFF	OFF	ON	OFF	ON	ON	OFF
234	EA	OFF	OFF	OFF	ON	OFF	ON	OFF	ON
235	EB	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
236	EC	OFF	OFF	OFF	ON	OFF	OFF	ON	ON
237	ED	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF
238	EE	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
239	EF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
240	F0	OFF	OFF	OFF	OFF	ON	ON	ON	ON
241	F1	OFF	OFF	OFF	OFF	ON	ON	ON	OFF
242	F2	OFF	OFF	OFF	OFF	ON	ON	OFF	ON
243	F3	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
244	F4	OFF	OFF	OFF	OFF	ON	OFF	ON	ON
245	F5	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
246	F6	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON
247	F7	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
248	F8	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
249	F9	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF

ID Node Number Lookup Table

ID NO.		POSITION							
DEC	HEX	0	1	2	3	4	5	6	7
250	FA	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON
251	FB	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
252	FC	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
253	FD	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
254	FE	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
255	FF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF